YAMAHA LSI's:

V9990

(E-VDP-III)

■ GENERAL DESCRIPTION

The V9990 is a Video Display Processor (VDP) with the following features:
High-speed drawing and animation functions,
multiple screen modes *(for games, AV, and OA purposes),*
multi-type monitor support - *CRT-TV-sets, PC CRT-monitors, and LCD panels.*

■ FEATURES

Game Specifications:

For this type, there are two pattern display modes as follows.

- **P1 (Display resolution 256 × 212 2 screens)**
- **P2 (Display resolution 512 × 212)**

Various highly advanced functions are available such as powerful sprite function and omnidirectional scroll function.

AV Specifications

For this type, there are four kinds of bitmap display modes which can be displayed on an NTSC or PAL monitor as follows.

- o B1 (Display resolution 256 x 212)
- o B2 (Display resolution 384 x 240)
- o B3 (Display resolution 512 x 212)
- o B4 (Display resolution 768 x 240)

- o Capable of doubling the vertical resolution through interlacing.
- o Can display up to 32768 colours/dot.
- o Built in colour palette *(64 colours selected out of 32768).*
- o Omnidirectional smooth scrolling.
- o Superimposition and digitization.

- Allows expanded 4-directional use of the monitor screen display range by using the over-scan modes (B2, B4) in applications such as for teleprompt operation. *(telopper)*
- High-speed hardware drawing commands, such as: screen transfer, colour lines and colour font development.
- Hardware display cursor.

OA Specifications

For this type of application, there are two kinds of bitmap display modes which can be displayed on a High resolution monitor as follows.

- B5 (Display resolution 640 x 400)
- B6 (Display resolution 640 x 480)

- Can display up to 16 colours/dot. *(selectable out of 32768 colours depending on the colour palette)*
- Omnidirectional smooth scrolling.
- High-speed hardware drawing commands, such as: screen transfer, colour lines and colour font development.
- Hardware display cursor.

Misc. features

- Built-in Digital-to-Analog converter
- Linear RGB output
- Direct connection of CG ROM such as a Kanji ROM is possible.
- VRAM configurations:

64Kb x 4
128Kb x 8 } Dual port DRAM *(the access time is 120nS, but 100nS is achievable in B6-mode.)*
256Kb x 4

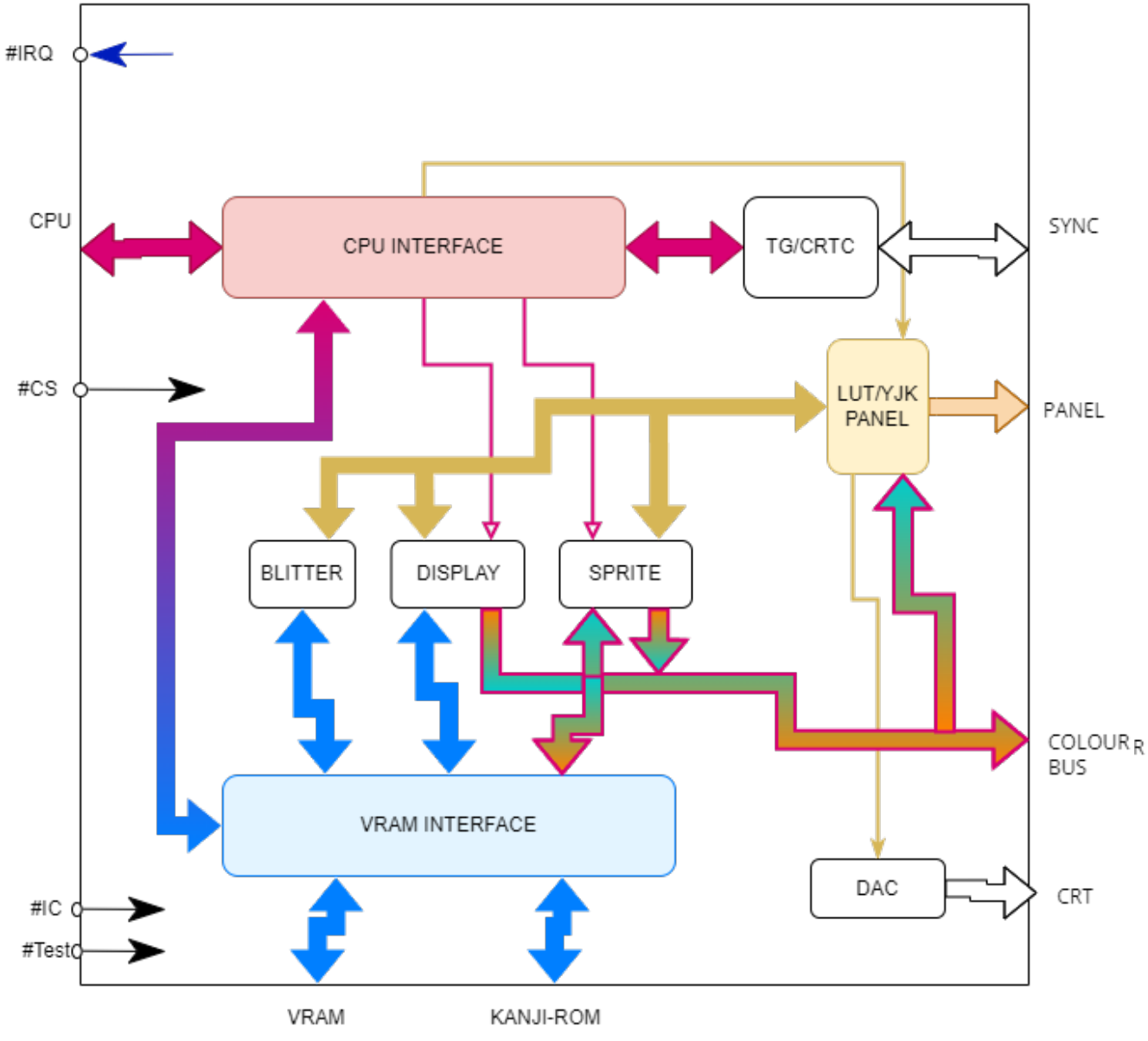
Capacities of 128KB, 256KB and 512KB is possible to achieve. (how?)

- Direct-memory access from CPU to VRAM by means of the 16-bit bus.
- LCD-panel compatibility (1 panel full drive, or 2 panels but with single drive)

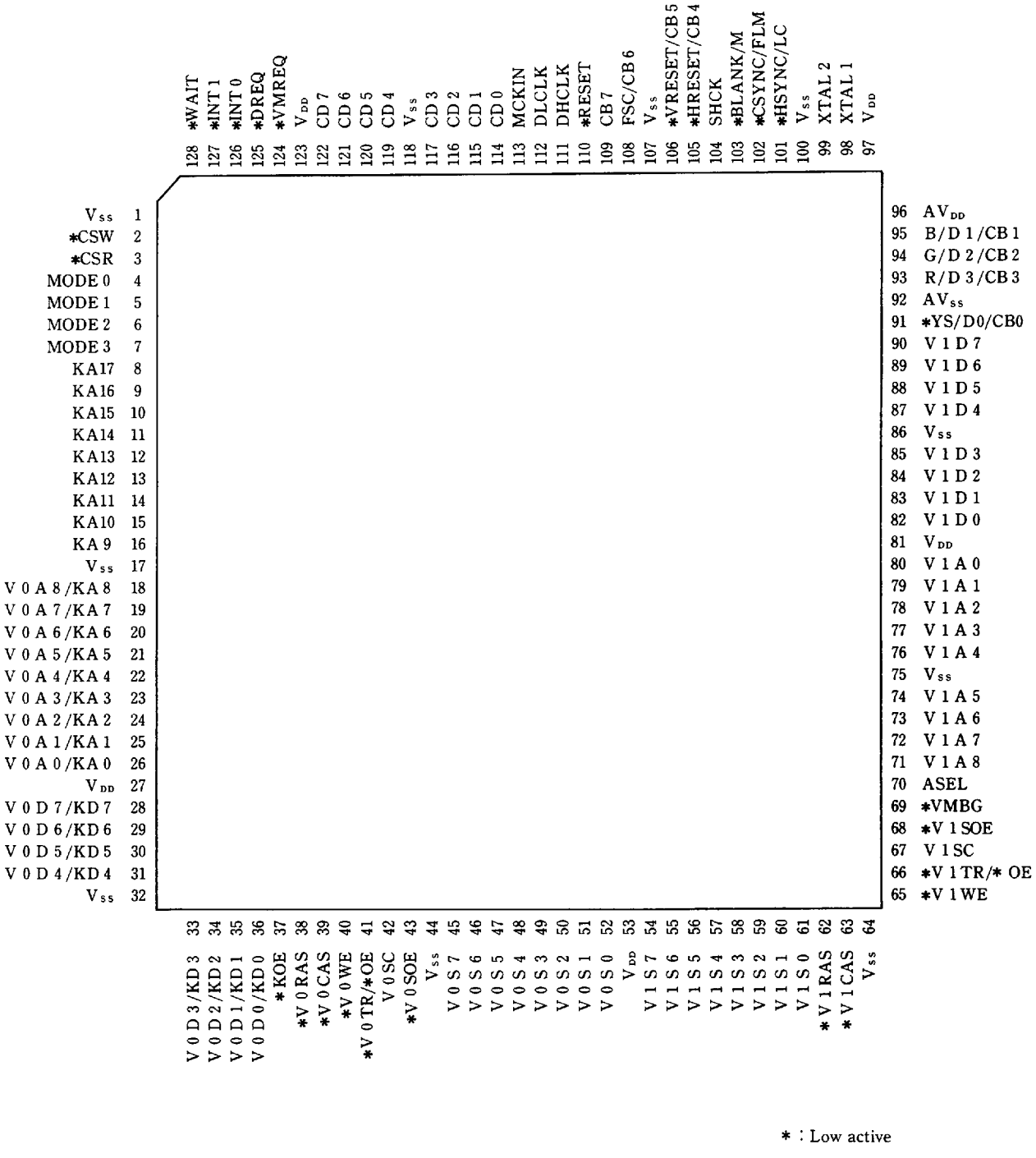
■ BLOCK DIAGRAM

YAMAHA V9990

Enhanced VDP Chip
Block Diagram



■ PIN ASSIGNMENT



* : Low active

■ DESCRIPTION OF TERMINALS

1) CPU Interface

- CD7-0 (I/O)
  8-bit bidirectional data bus of CPU.
- MODE3-0 (I)
  Address for I/O port selection of CPU. Select P#0 to P#F of VDP.
- *CSR (I)
  CPU read signal which is chip-selected for VDP. VDP outputs data to CD7-0 when this signal is active (Low).
- *CSW (I)
  CPU write signal which is chip-selected for VDP. D7-0 data is set to VDP at the rise of this signal.
- *WAIT (O : Open drain output)
  Wait signal to CPU. This signal becomes active (Low) while VDP is busy when reading or writing is executed from CPU.
- *INT1, *INT0 (O : Open drain output)
  This signal becomes active (Low) when the interrupt condition exists in VDP. The interrupt condition can be obtained by reading P#6 and cancelled by writing "1" as an interrupt condition corresponding to P#6.
  INT0 is an interrupt for vertical retrace line interval and at command end.
  INT1 is an interrupt for display position.
- *DREQ (O : Open drain output)
  Data request signal. This signal becomes active (Low) when data ready occurs while command is executed and can be cancelled by means of P#2 access.
- *VMREQ (I)
  This signal becomes active (Low) when CPU makes an access to VRAM without using VDP. VDP activates the WAIT signal till access to the VRAM becomes possible. Following that, it makes the VMBG signal active and releases the data bus, address bus and WE signal of VRAM0 and VRAM1.

2) VRAM Interface

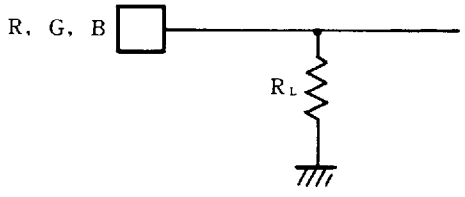
- *KOE (O)
  Data output enable signal for Kanji ROM. The data bus (V0D7-0) is used by both VRAM0 and kanji ROM and when this signal is active (Low), kanji ROM data bus becomes valid.
- KA17-9 (O)
  Address bus (A17-9) output of Kanji ROM.

- V0A8-0/KA8-0 (O : 3 state output)
  Address bus output of VRAM0. When *KOE is active, Kanji ROM address bus output becomes valid.
- V1A8-0 (O : 3 state output)
  Address bus output of VRAM1.
- V0D7-0/KD7-0 (I/O)
  Bidirectional data bus of VRAM0 RAM port. When *KOE is active, Kanji ROM data bus input becomes valid.
- V1D7-0 (I/O)
  Bidirectional data bus of VRAM1 RAM port.
- V0S7-0, V1S7-0 (I)
  Data bus input of VRAM0, VRAM1 serial port.
- *V0RAS, *V1RAS (O)
  Low address strobe signal output of VRAM0 and VRAM1.
- *V0CAS, *V1CAS (O)
  Column address strobe signal output of VRAM0 and VRAM1.
- *V0WE, *V1WE (O : 3 state output)
  Write strobe signal output of VRAM0 and VRAM1.
- *V0TR/*OE, *V1TR/*OE (O)
  Data transfer control signal of VRAM0 and VRAM1 or data output enable signal of RAM port.
- V0SC, V1SC (O)
  Serial clock signal output of VRAM0 and VRAM1.
- *V0SOE, *V1SOE (O)
  Data enable signal of VRAM0 and VRAM1 serial port.
- *VMBG (O)
  When this signal is active (Low), VDP releases VRAM0, VRAM1 data bus, address bus and WE signal (resulting in high impedance).
- ASEL (O)
  Low address timing signal for VRAM when making an access to VRAM from outside.

3) **CRT and Panel Interface**

- *HSYNC/LC (O)
  Horizontal synchronous signal output (without equivalent pulse). Panel latch clock signal output when VDP is in panel mode.

- *CSYNC/FLM (O)
  Combined synchronous signal output (with equivalent pulse). Panel scanning start signal output when VDP is in panel mode.
- *BLANK/M (O)
  This signal becomes active (Low) while retrace line blanking interval. Panel AC conversion signal output when VDP is in panel mode.
- SHCK (O)
  Panel shift clock signal output.
- R, G, B, *YS/D3-0/CB3-0 (O)
  Linear RGB output and YS signal output. Panel data output or color bus output when in panel mode. YS signal becomes active (Low) when VDP data is superimposed.



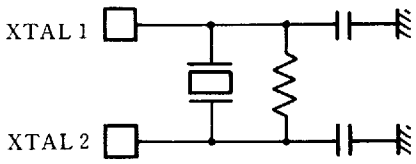
- *HRESET/CB4 (I/O)
  Internal horizontal timing is initialized when this signal falls. It is possible to synchronize with other VDP but when horizontal cycle differs, normal operation of VDP is not assured. Color bus output becomes valid when in panel mode.
- *VRESET/CB5 (I/O)
  Internal vertical timing is initialized when this signal falls. It is possible to synchronize VDP from outside. Color bus output becomes valid when in panel mode.
- FSC/CB6 (output)
  NTSC-standard 3.58 MHz clock (subcarrier). The C-bus output becomes valid when in LCD-panel mode.
- CB7 (O)
  Color bus output. CB7-0 data is output as follows.

Mode	Dot Clock	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	CB Clock
P1	5MHz	—	—	CC5	CC4	CC3	CC2	CC1	CC0	DLCLK
P2	10MHz	—	—	CC5	CC4	CC3	CC2	CC1	CC0	DHCLK
8B/D	7, 10MHz/ 5MHz	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	DHCLK/DLCLK
4B/D	25, 21MHz/14MHz	ECC3	ECC2	ECC1	ECC0	OCC3	OCC2	OCC1	OCC0	DHCLK
4B/D	7, 10MHz/ 5MHz	—	—	—	—	CC3	CC2	CC1	CC0	DHCLK/DLCLK
2B/D	25, 21MHz/14MHz	—	—	ECC1	ECC0	—	—	OCC1	OCC0	DHCLK
2B/D	7, 10MHz/ 5MHz	—	—	—	—	—	—	CC1	CC0	DHCLK/DLCLK

Note) B/D : Bit/Dot, ECC3-0 : CC3-0 of even number dot, OCC3-0 : CC3-0 of odd number dot

4. CLOCK SIGNALS

o XTAL 1 (input), XTAL 2 (output)
Terminals for 21 MHz (MCK) crystal oscillator. XTAL1 is used when inputting externally oscillated clock.

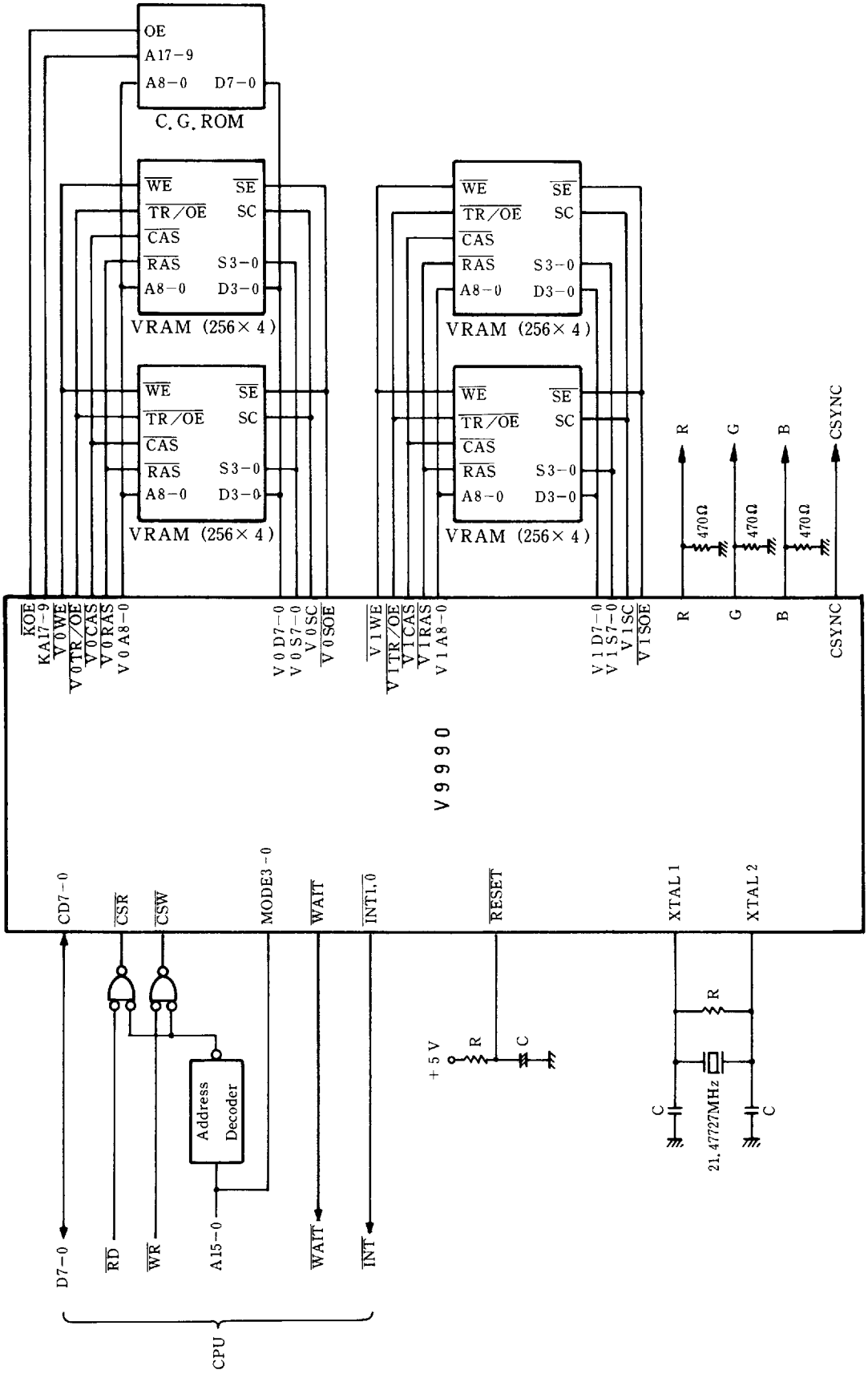


- MCKIN (I)
  14MHz clock (MCK) input. Use VDP internal register when selecting XTAL or MCKIN.
- DHCLK, DLCLK (O)
  Dot clock output. 1/2MCK for DHCLK and 1/4MCK for DLCLK.

5) Others

- *RESET (I)
  VDP is initialized when this signal is active (Low). All registers (except LUT) will be "0" cleared.
- AVDD, AVSS (I)
  Analog power supply input for RGB.
- VDD, VSS (I)
  Digital power supply input.

■ SYSTEM CONFIGURATION



■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage (V_{DD})	−0.3 ~ +7.0V
Input voltage (V_I)	−0.3 ~ V_{DD} +0.3V
Output voltage (V_O)	−0.2 ~ V_{DD} +0.3V
Storage temperature (Tstg)	−50 ~ +125°C

Recommended operating conditions

Symbol	Item	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	4.75	5.00	5.25	V
V_{SS}	Supply voltage		0		V
V_{IL1}	Low level input voltage (Group 1)	−0.3		1.5	V
V_{IH1}	High level input voltage (Group 1)	3.5		V_{DD}	V
V_{IL2}	Low level input voltage (Group 2)	−0.3		0.8	V
V_{IH2}	High level input voltage (Group 2)	2.2		V_{DD}	V
T_{op}	Operational temperature	0		70	°C

Group 1 : XTAL1, MCKIN
Group 2 : Input terminals other than group 1

Electrical characteristics under the recommended operating conditions

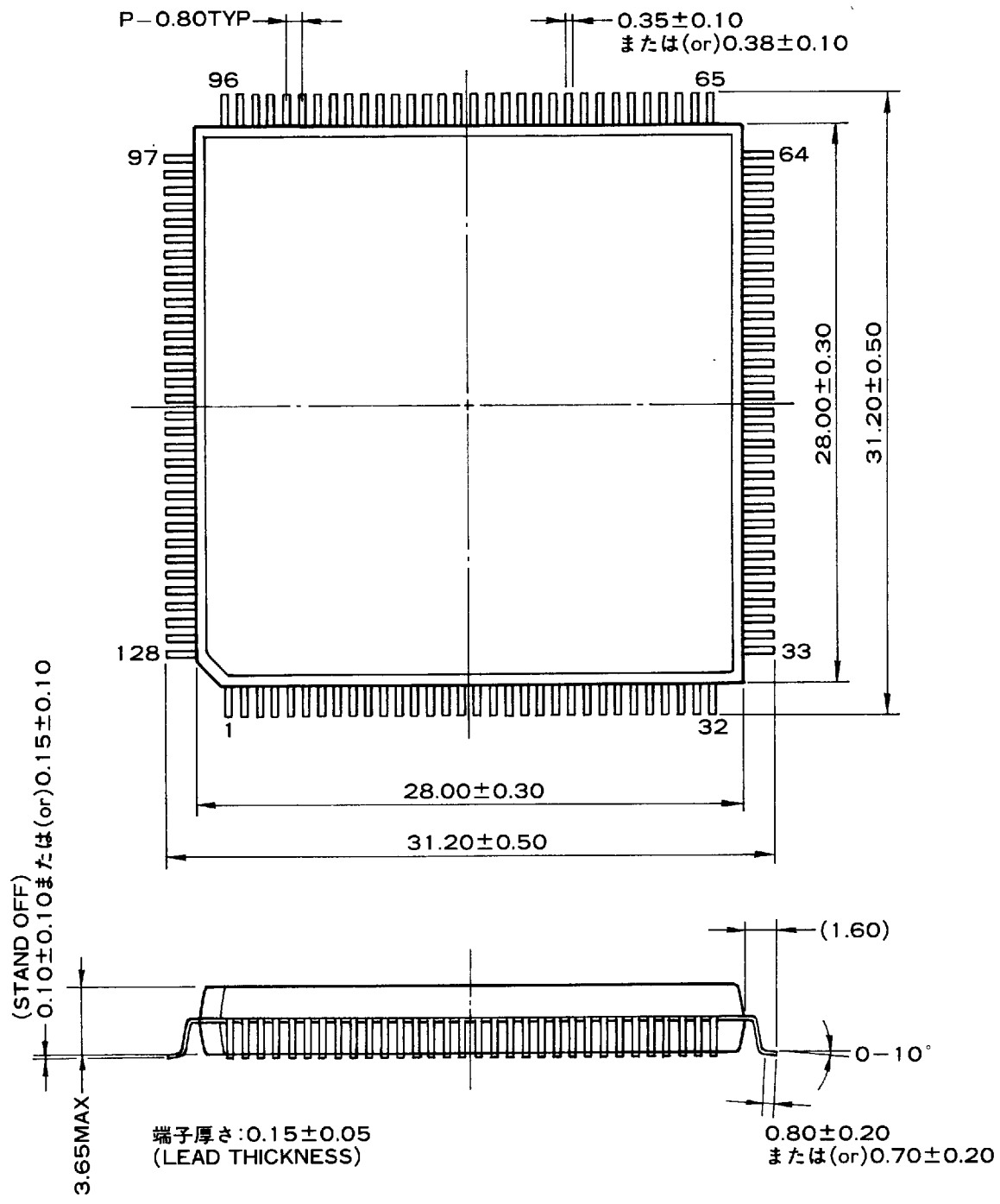
DC characteristics

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	I_{OL} = 1.6mA			0.4	V
V_{OH}	High level output voltage (except OPEN DRAIN terminal)	I_{OH} = −0.1mA	2.7			V
I_{LI}	Input leak current				10	μA
I_{LO}	Output leak current				25	μA
I_{DD}	Power consumption			100	140	mA

Terminal capacitance

Symbol	Item	Min.	Typ.	Max.	Unit
C_I	Input terminal capacitance			8	pF
C_O	Output terminal capacitance			10	
C_{IO}	Input/output terminal capacitance			12	

■ EXTERNAL DIAGRAM OF THE PACKAGE



UNIT : mm

The specifications of this product are subject to improvement changes without prior notice.

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