4.0 CPU/VDP INTERFACE

The VDP interfaces with the 99XX CPU via a bidirectional 8 bit port, controlle by one mode or address line and two chip select lines. Figure 4-1 shows a block diagram of the VDP port. Figure 4-2 shows the VDP/CPU Parallel Interface and defines the states of the Mode Control Signals. Details of the 9948 can be found in Appendix D.

FIGURE 4-1 CPU/VDP/MEMORY INTERFACE

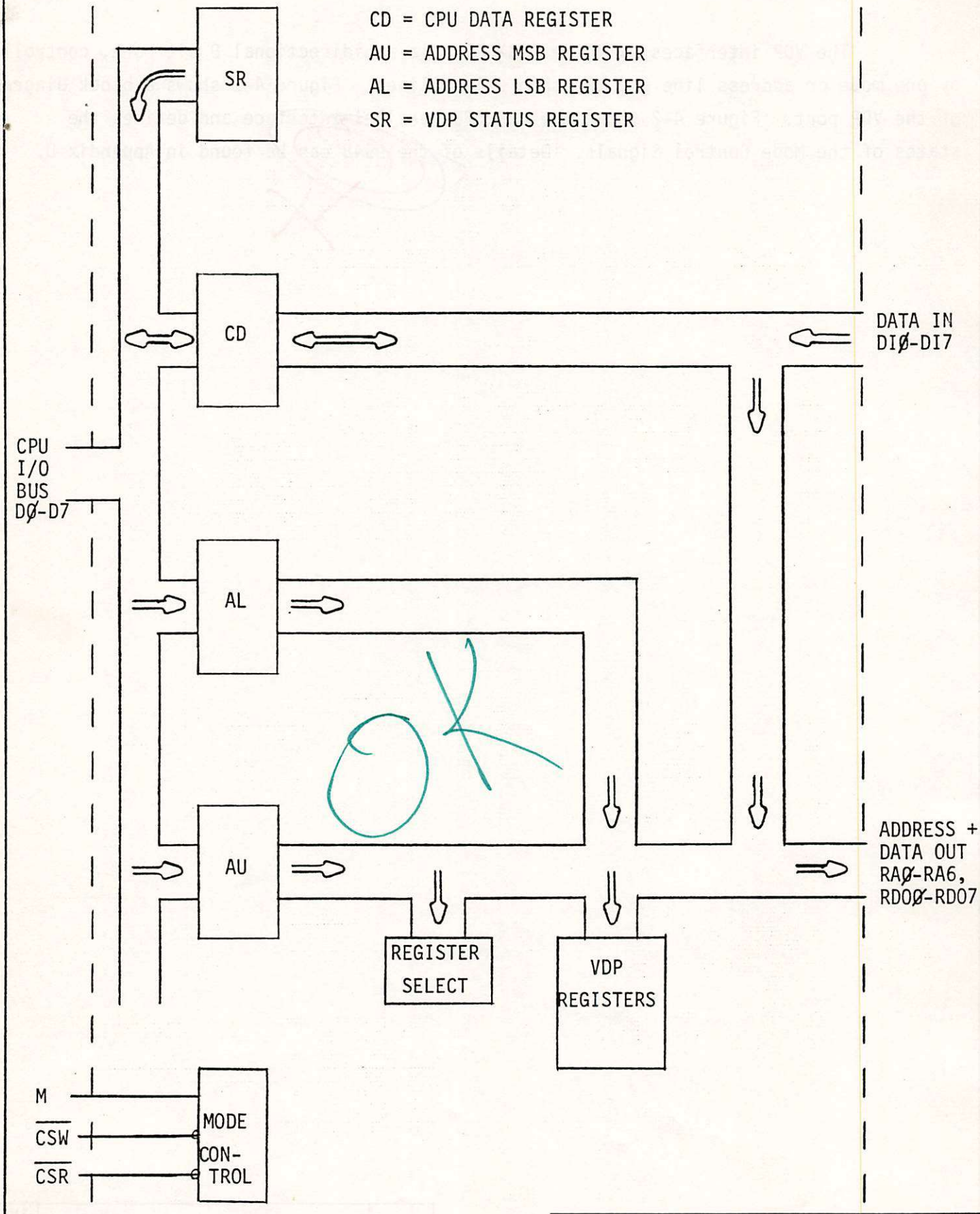


TABLE 4-1 VDP - CPU BUS CONTROL

		MODE DEFINITION		
		$\overline{CSW}$	$\overline{CSR}$	MODE
WRITE TO RAM				
MODE 2	Address LSB	0	1	1
MODE 2	Address MSB, MSB=0, $\overline{R/W}$=1	0	1	1
MODE 0	Write Data	0	1	0
WRITE TO VDP				
MODE 2	Data	0	1	1
MODE 2	MSB=1 $\overline{R/W}$=X, 3 LSBs=Register Number	0	1	1
READ FROM RAM				
MODE 2	Address LSB	0	1	1
MODE 2	VDP=0, $\overline{R/W}$=0 Address MSB	0	1	1
MODE 1	Read Data	1	0	0
READ FROM VDP				
MODE 3	Read Status	1	0	1

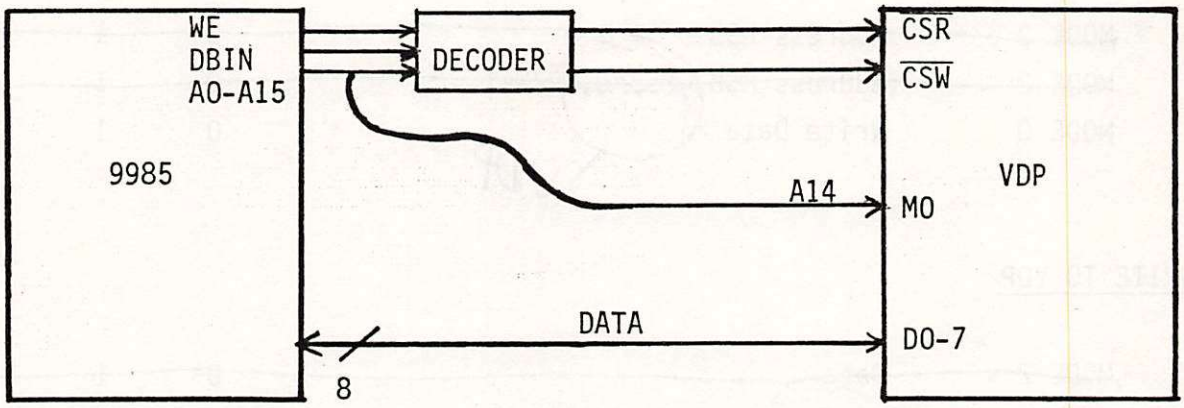


FIGURE 4-2 VDP PARALLEL INTERFACE

MODE CONTROL

MODE 0	Request to write data from I/O lines to VDP RAM; clears byte flag *.
MODE 1	Request to read data from VDP RAM to I/O lines; clears byte flag *.
MODE 2	Byte Flag Cleared: Load data on I/O lines to LSB; set byte flag. Byte Flag Set: Load data on I/O lines to MSB; clear byte flag.
MODE 3	Read Status from VDP; clears byte flag.

* Address is incremented following memory cycle.

** Reset also clears byte flag

4.1 VDP ADDRESSING

Initial video display systems using the VDP will use only 4K bytes of the total 16K possible to be addressed. It is envisioned, however, that follow-on systems will use 16K Dynamic RAMs utilizing the $\overline{RAS}$ - $\overline{CAS}$ addressing technique. (Note: The VDP Memory Controller will also control the refresh operations necessary for the dynamic RAMs). Figure 4-3 shows an example memory address layout. Figure 4-4 shows a diagram to allow up to 16K of RAM using bank switching of 4K DRAMs.

In addition, 8 bytes of address space have been reserved for VDP registers (see Figure 4-5). These VDP registers contain the command and status registers, and the various base address registers used by the VDP to form display data address. Appendix B describes the concatenation of the various display data elements and the contents of the base registers to form the 14 bit address necessary to access the data in the display memory.

misleading

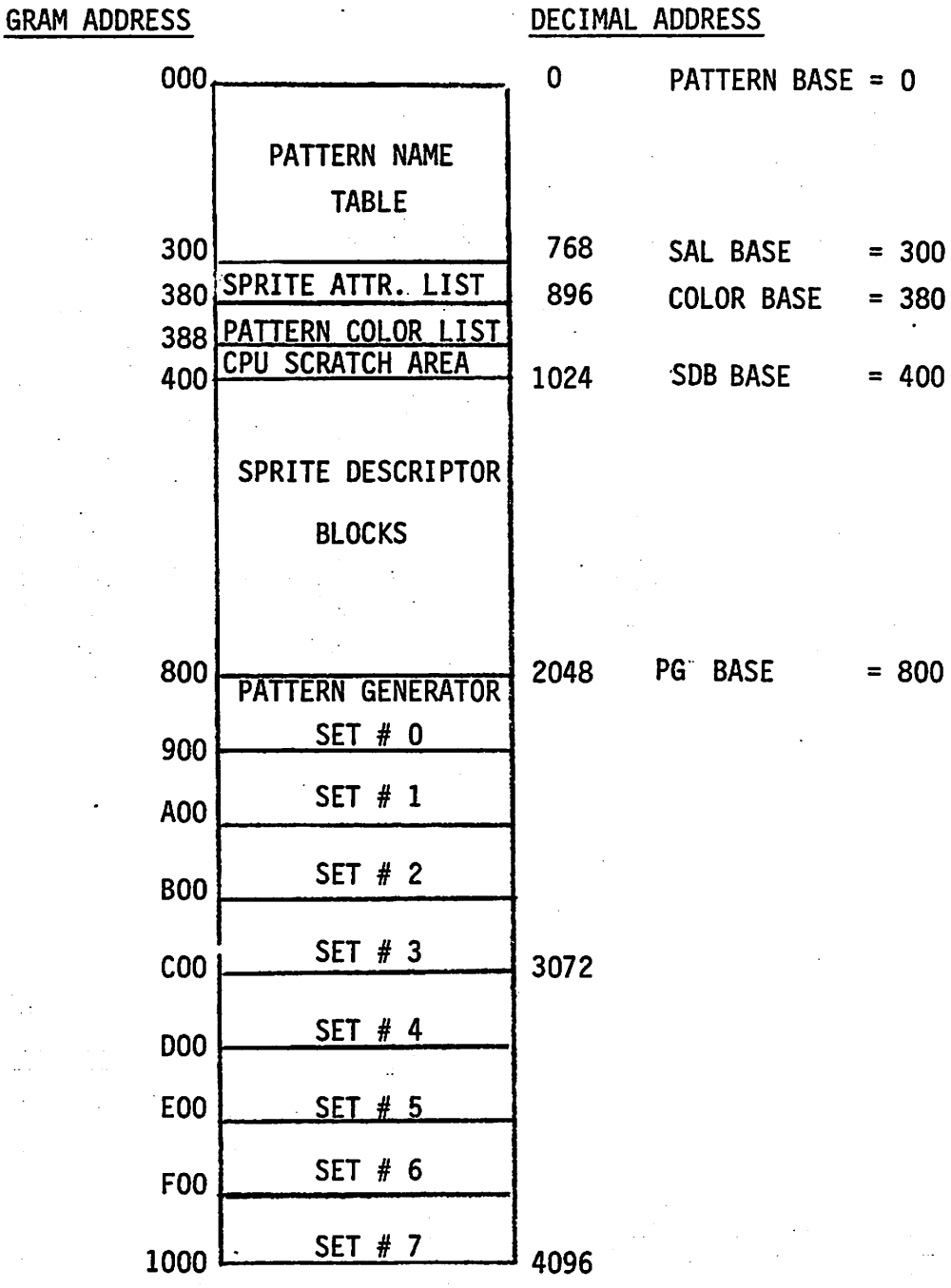
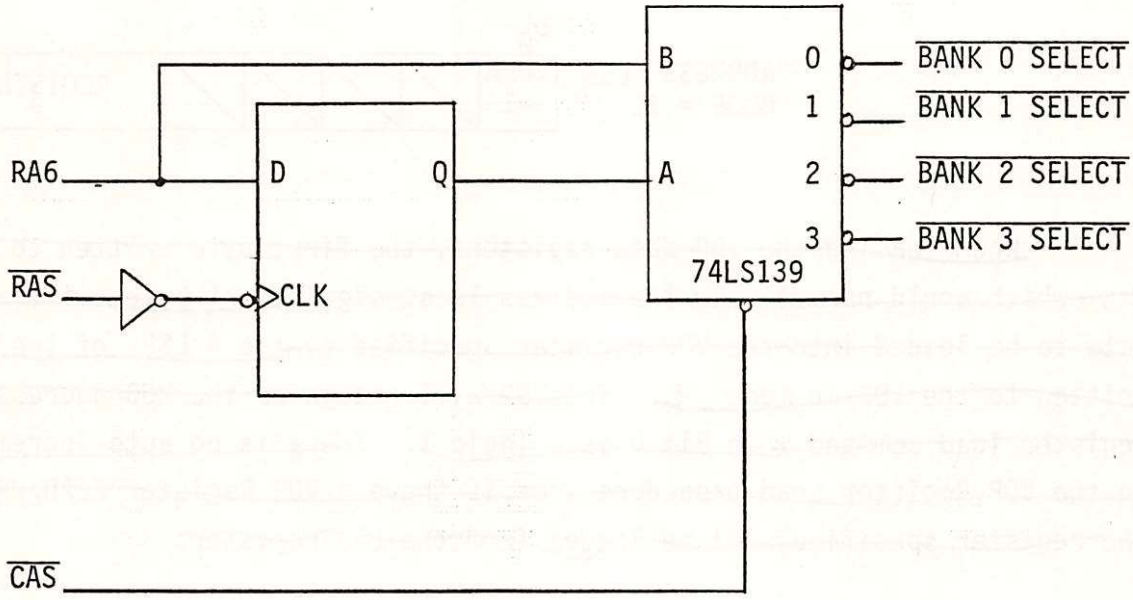
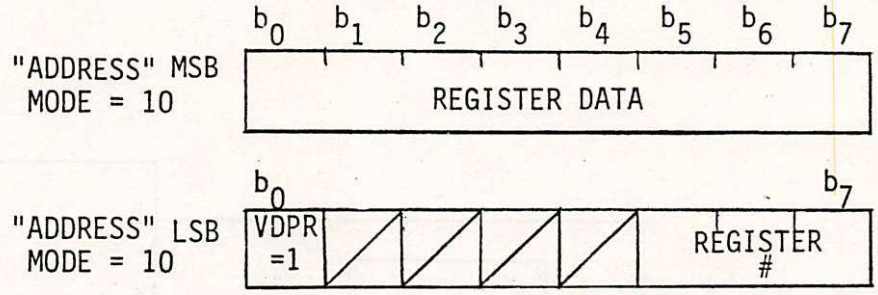


FIGURE 4 - 3 EXAMPLE MEMORY ORGANIZATION

FIGURE 4-4 BANK SWITCHING OF 4K DRAMs



4.2 LOADING VDP REGISTERS



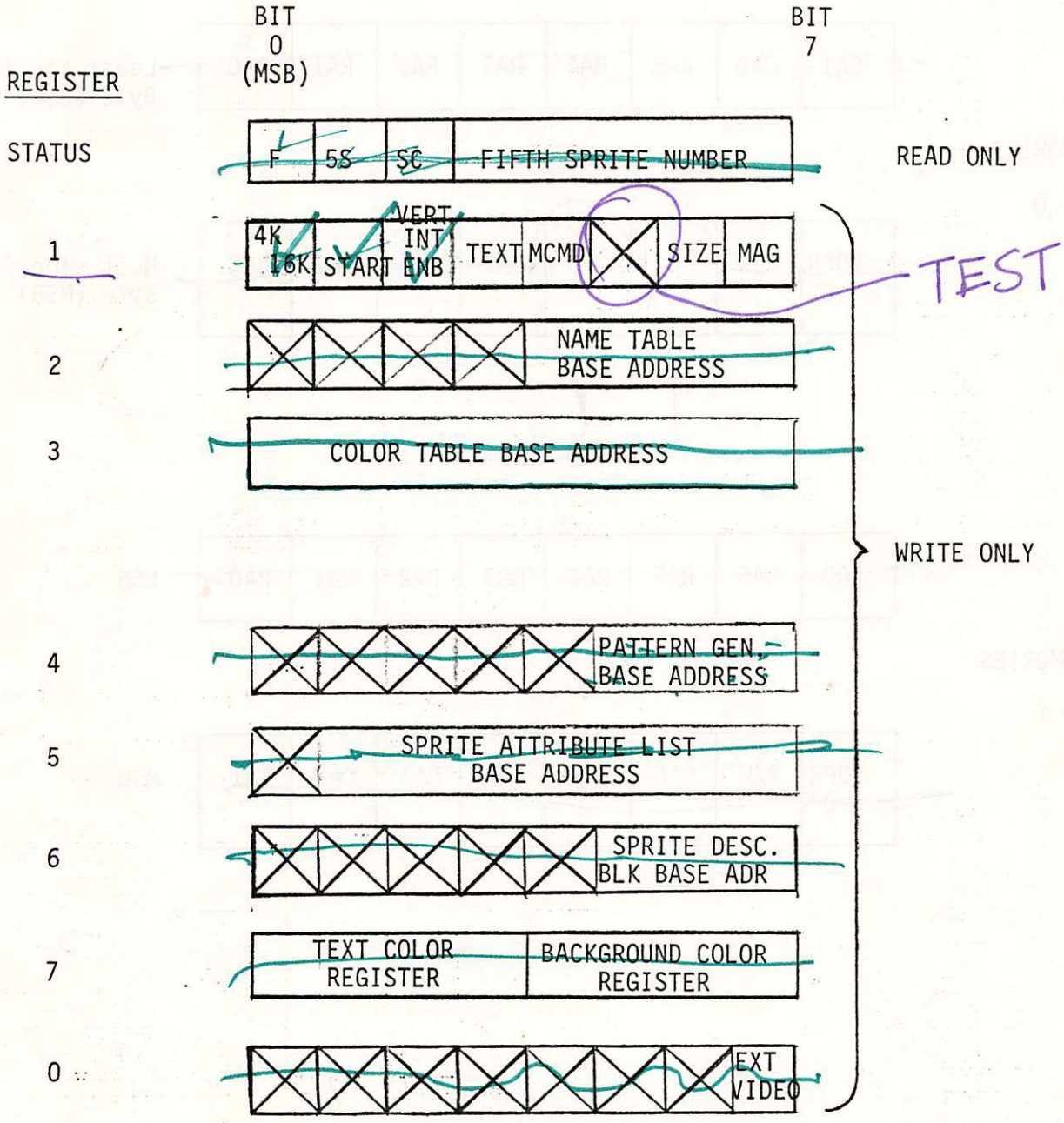
When loading the VDP data registers, the first byte written to the VDP in mode 2, which would normally be the address least significant byte, will actually be the data to be loaded into the VDP register specified by the 4 LSBs of the second byte written to the VDP in mode 2. The VDP will recognize the MSB address byte as a VDP register load command when Bit 0 is a logic 1. There is no auto-increment capability in the VDP Register Load procedure, nor is there a VDP Register READ/WRITE indicator. The register specified will be loaded from the LSB register.

4.3 READING THE VDP STATUS REGISTER

The status register will be made available to be read with the Read Status (mode 3) command. This register provides the frame interrupt, fifth sprite, and sprite coincidence status flags in addition to the fifth sprite number.

4.4 VDP ADDRESS REGISTER OPERATIONS

Two eight bit transfers are required to load a 14 bit address into the VDP Memory Address Register. This is accomplished by transferring the least significant byte of the address from the CPU to the VDP via the bus in mode 2 followed by the most significant byte, again in mode 2. Figure 4-6 shows the bit assignments for addressing 4K or 16K dynamic RAMs.

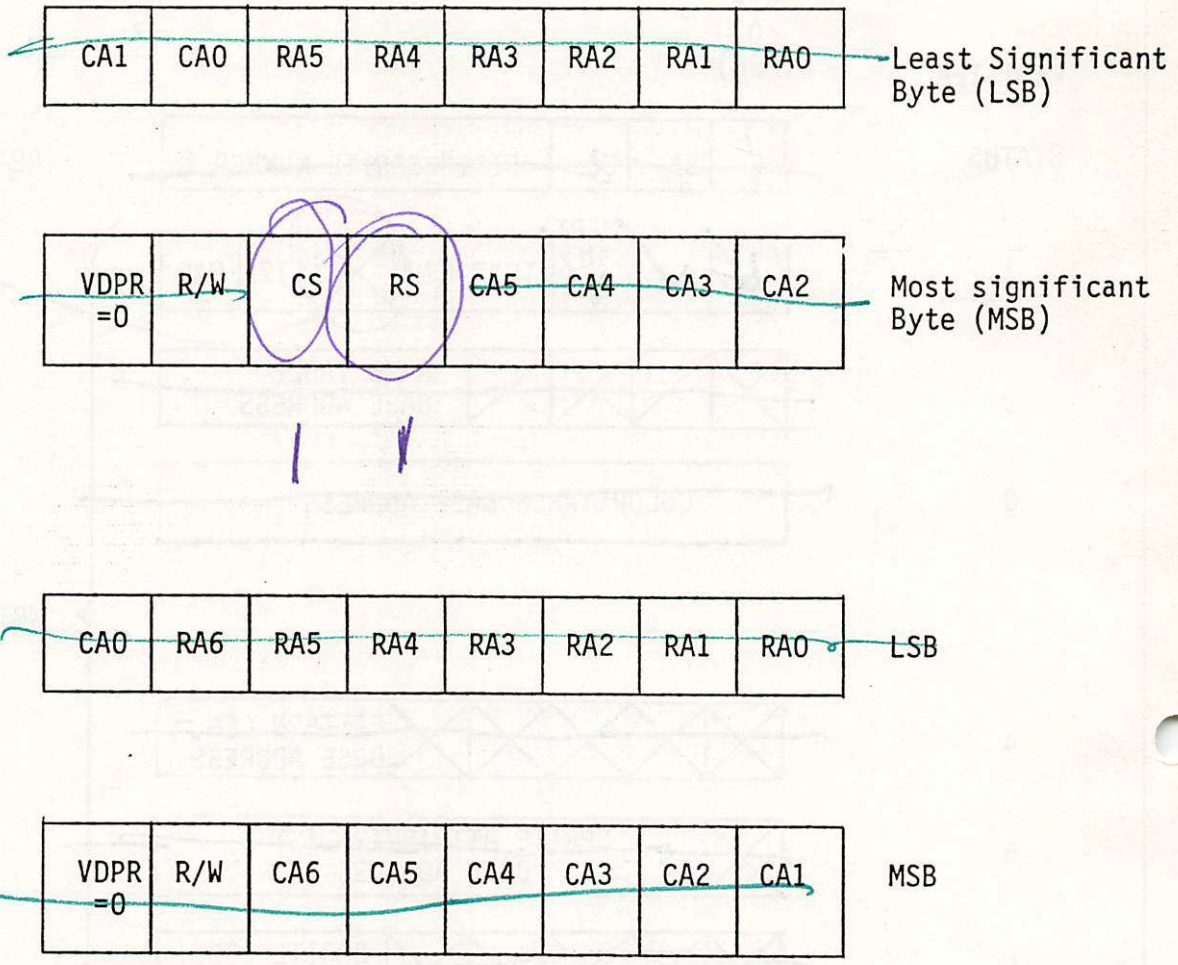


Unused bit - should be set to a "0" value to maintain compatibility with future versions of the VDP

FIGURE 4 - 5 VDP REGISTER ASSIGNMENT

TI-11338C

FIGURE 4 - 6 4K/16K DRAM ADDRESS BIT ASSIGNMENTS



4.5 MEMORY ACCESS - WRITE

WRITE ADDRESS LSB
MODE 2

WRITE ADDRESS MSB
MODE 2

WRITE DATA
MODE 0

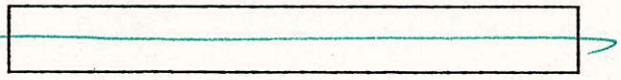
WAIT

WRITE DATA
MODE 0

The operations shown on the preceeding page detail the steps required to write data from the CPU to the display RAM. The VDPR bit is reset to 0, indicating access to RAM is requested, and the R/W bit has been set to 1 to identify the requested operation as a WRITE operation. In the RAM access mode of operation, the VDP automatically increments the address register after the byte has been written to set up the VDP for the next byte. (Approximate memory latency 8.0 µs).

4.6 MEMORY ACCESS - READ

WRITE ADDRESS LSB
MODE 2

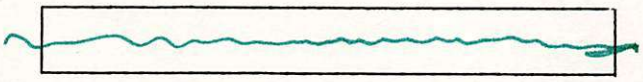


WRITE ADDRESS MSB
MODE 2

READ DATA
MODE 1

(WAIT)

READ DATA
MODE=1



The operations shown on the precceding page detail the steps required to read sequential data from the display RAM. R/W is set to 0 indicating read operations and the next memory address is set up when the current data is read.

4.7 STATUS FLAG OPERATION

Three internal status flags govern the operation of the VDP in memory and register access control - MEMRQ, MEMWR, and BYTE.

A READ DATA operation (MODE) sets MEMRQ for the next READ operation. A WRITE DATA operation (MODE) sets MEMRQ and MEMWR. Upon completion of all memory action initiated by MEMRQ, MEMRQ will be reset by the VDP. The byte flag is used to determine whether to load the CPU bus in Mode 2 to the LSBs or MSBs of the CPU address register. It is set by the first Mode 2 operation and cleared by the next Mode 2, any other CPU operation, or reset. Following a CPU memory access the memory address is incremented.

4.8 VDP RESET OPERATIONS

Since the order of loading the memory address and VDP control registers is critical in terms of data identification, it is important that the device operation be started from a known state. A low active signal applied to the $\overline{\text{RSET}}$ pin must last for at least 2 µs and will establish these known conditions, in anticipation of device and memory initialization. Reset does the following: Synchronizes all clocks to its negative going edge (this includes ϕ_1 - ϕ_4 Control Clocks, CPUCLK, GROMCLK and Color Burst), sets horizontal and vertical counters to known state, clears the command register, sets the text color and border color to black (so that initially black is displayed) and clears all CPU status flags.

During operation, resetting the START bit will inhibit display and the device will function as though it were in the vertical retrace period of screen operation. (i.e., memory is refreshed and CPU has all other memory accesses available). Display will continue when START is set again.

5.0 STATUS REGISTER

5.1 INTERRUPT OPERATION

The F status flag in the status register is set to a logic one at the end of the vertical active display interval. It is cleared to zero after the status register is read (2 μs following $\overline{CSR}$ going inactive) or by the reset. If the interrupt enable bit in the command register is a logic one, then the VDP interrupt output ($\overline{INT}$) is active (low) whenever the F status flag is a logic one.

5.2 COINCIDENCE

The C status flag in the status register is set to a logic one whenever two or more sprites "coincide" (have active "1" dots at the same location). The C status flag is cleared to zero after the status register is read or be reset.

MSB

0	1	2	3	7
F	5S	C	5S #	

STATUS REGISTER

FIGURE 5-1 STATUS REGISTER

5.3 FIFTH SPRITE

The 5S status flag in the status register is set to a logic one whenever there are five or more sprites on a horizontal line (0 to 192) and the frame flag is equal to a logic zero. The 5S status flag is cleared to zero after the status register is read or by a reset. The number of the fifth sprite is placed into the lower 5 bits of the status register when the 5S flag is set and is valid whenever the 5S flag is a logic one.

5.4 STATUS REGISTER ACCESS

The status register may be read at any time in order to test the C and 5S status bits; asynchronous reads will, however, cause the frame flag bit to be reset and therefore missed. Consequently, the status register should be read only when the VDP interrupt is pending.