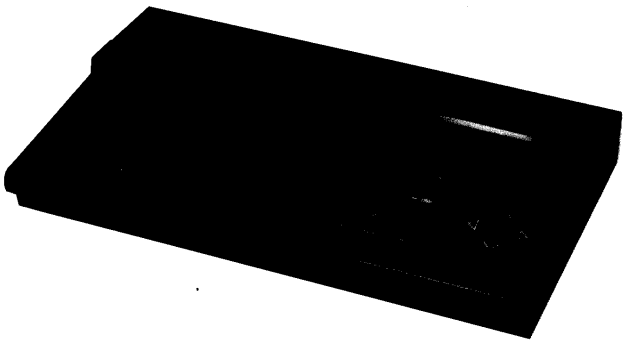
HB-55P/75P/75B

SERVICE MANUAL



HOME COMPUTER

SONY®

TABLE OF CONTENTS

CHAPTER 1
OPERATION

1-1. FEATURES

Possible to connect any monitor TV
The HB-55P/75P/75B has an RF connector and a 6-pin DIN-type VIDEO/AUDIO connector for video/audio output. In addition to this, the HB-75P/75B has an analog RGB connector, so that any type of monitor TV can be connected to the computer.

Various graphic patterns and characters input
Combinations of normal alphanumeric keys and control keys allow you to easily input up to 252 kinds of characters, symbols and graphic patterns from the keyboard.

Built-in MSX-BASIC
The built-in MSX-BASIC has 119 commands which allow you easy program development. With the MSX-BASIC sprite function, you can make and move the different patterns on each of the 32 sprite planes.
The sound generator makes it possible to output three tones and one noise simultaneously, so that you can generate various effect sound or music by using the PLAY and SOUND command of the MSX-BASIC.
Two supplied manuals for the MSX-BASIC will tell you not only how to use the MSX-BASIC but also the pleasure of programming.

Easy-to-use Personal Data Bank
The Personal Data Bank, which is the other built-in software, makes it easy to handle personal data such as addresses, phone numbers, and so on. Convenient to use, you are sure to find many uses for it.

Various peripherals for the HB-55P/75P/75B
Various peripherals can be connected: MSX-BASIC program and data and the Personal Data Bank data can be saved on an audio cassette tape, a data cartridge, or a micro floppydisk. To print out data or graphics, the color plotter printer is useful. When playing a computer game, you can use up to two joystick controllers to make the game more exciting.

Peripheral devices for HB-55P/75P/75B

Device name	Major features
HBD-50 Micro Floppydisk Drive	• High-density information storage • Easy-to-operate • Fast recall of data
JS-55 Joystick	• Designed for left- or right handed players • Shoot buttons on both left and right
JS-75 Wireless Joystick	• No cords to get tangled • Can be operated from up to 7 meters away
TCM-3000D Datacorder	• Easy to operate with any computer • High-speed data transfer
PRN-C41 Color Plotter Printer	• Four-color printer: black, blue, green and red • Light weight and compact • Can use any paper up to 114mm in width

1-2. SPECIFICATIONS

CPU

Processor used	Z-80A
Clock frequency	3.579545 MHz
WAIT	1 WAIT at CPU M1 cycle
Interrupt	Maskable interrupt Z-80A mode 0 mode 1 mode 2
Resetting	Automatic at power on/Manual (Memory contents are not saved.)

Memory

Main memory	HB-55P 16K bytes RAM Expansion is possible up to 32K bytes or 64K bytes with Sony Expansion Memory Cartridge HBM-16/HBM-64. HB-75P/75B 64K bytes RAM
ROM	48K bytes MSX-BASIC: 32K bytes Utility Program: 16K bytes

CRT display

CRT controller	TMS9929ANL
Display screen	Character display, graphic display and border area
Character display	8×8 dot matrix/character 37 characters×24 lines, 16 colors (max. 40×24) (The initial state in MSX-BASIC is set to this mode.)
Graphic display	16 colors Graphic I·II 256 (horizontal) ×192 (vertical) dots Multi-color 64 blocks (horizontal) ×48 blocks (vertical) Sprite function Number of sprite plane: 32
Border area	16-color display
Output interface	PAL video output: composite video signal 1 V p-p, 75 ohms, sync negative RGB video output: RGB analog signal, 0–0.7 V, RF signal: TV UHF 36 ch Audio output: −5 dBs

I/O interface

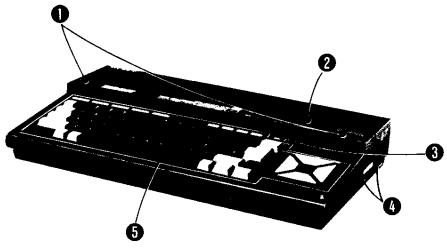
Keyboard	Software scanning Total number of keys: 73 (HB-55P) 74 (HB-75P/75B) Control keys: 11 (HB-55P) 12 (HB-75P/75B) Function keys: 5 Edit keys: 8
Audio cassette interface	8-pin DIN jack Baud rate: 1200/2400 bauds Baud rate is selectable with the CSAVE command or the SCREEN command of MSX-BASIC. Remote control function provided
Sound generator	8-octave, 3 tones and 1 noise output
Printer interface	14-pin connector TTL level Standard 8-bit parallel transfer
Joystick interface	9-pin connector (2)
MSX cartridge slot (2)	

General

Power requirement	HB-55P/75P 220 V ac ±10%, 50/60 Hz HB-75B 240 V ac ±10%, 50/60 Hz
Power consumption	24 W (main unit only)
Operating conditions	Temperature: 5°C to 35°C (41°F to 95°F) Humidity: 20 to 80%
Storage temperature	−15°C to +60°C (5°F to 140°F)
Dimensions	Approx. 405×67×245 mm (w/h/d) (16×2¾×9¾ inches) main unit only, including projecting parts and controls
Weight	Approx. 3.5 kg (7 lb 12 oz) main unit only
Accessories supplied	75-ohm coaxial cable (1) Cassette interface cable (1) Antenna selector (1) Receptacle for Cartridge slot B (1) Operating Instructions (1) How to use Personal Data Bank (1) Introduction to MSX-BASIC (1) MSX-BASIC Programming Reference Manual (1) Graphic pattern sheet (1) Graphic pattern decal (only HB-75P/75B) (1)

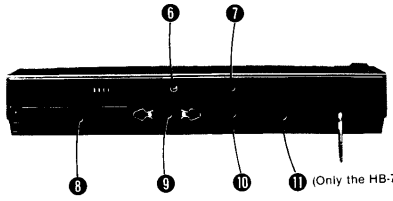
While the information given is true at the time of printing, small production changes in the course of our company's policy of improvement through research and design might necessarily be indicated in the specifications. We would ask you to check with your appointed Sony dealer if clarification on any point required.

1-3. LOCATION AND FUNCTION OF PARTS AND CONTROLS



(This photo is the HB-75P.)

Rear



(Only the HB-75P/75B)

❶ POWER switch and indicator
Press the switch to turn on the computer. To turn off, press the switch again. The indicator lights up while the power is on.

❷ Cartridge slot A
Accepts a ROM cartridge or a RAM cartridge here.

❸ RESET button
Press this button if there is a program overrun to reset the computer to the initial state. When the button is pressed, the built-in memory contents will be destroyed.

❹ CONTROLLER A and B connectors
Accepts joystick controllers. When using only one joystick controller, connect it to the CONTROLLER A connector.

❺ Keyboard
Is used to input the program and the data into the computer.

❻ RF (RF output) connector
When using a normal TV receiver, connect this connector to the TV antenna terminal with a 75-ohm coaxial cable.

❼ VIDEO/AUDIO (video/audio output) connector (6-pin DIN connector)
Connect to the monitor TV with a 6-pin DIN connector. This connector outputs both the video and the audio signals.

❽ Cartridge slot B
This slot can be used to insert a ROM cartridge or a RAM cartridge (an expansion memory cartridge, a game cartridge and so on) as the secondary slot. This slot is the same as cartridge slot A. Before using this slot, the receptacle should be installed.

❾ PRINTER connector (14-pin connector)
Connect an 8-bit parallel transfer printer with MSX specifications such as the Sony PRN-C41 color plotter printer.

❿ TAPE connector (8-pin DIN connector)
Connect to a tape recorder to save a program or data on a cassette tape or to load them into the computer from a tape.

⓫ RGB (RGB output) connector (21-pin connector)
The HB-55P is not equipped with this connector.
Connect to the monitor TV having an analog RGB input connector.

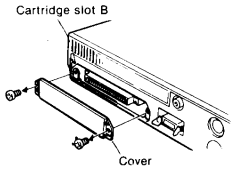
1-4. CONNECTION

Make sure to turn off the computer and all the devices to be connected.

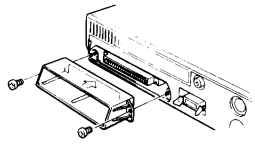
INSTALLING THE RECEPTACLE FOR CARTRIDGE SLOT B

When cartridge slot B is to be used, install the receptacle supplied.

1. Loosen the two screws, and remove the slot cover.



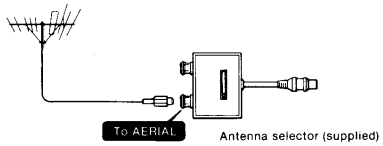
2. Fix the receptacle with screws.



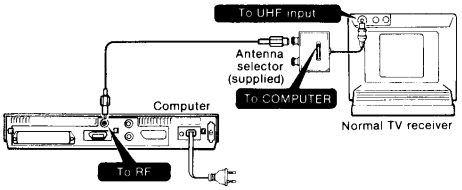
CONNECTING A MONITOR TV

Connecting a normal TV receiver

1. Connect the TV antenna terminal to the supplied antenna selector.



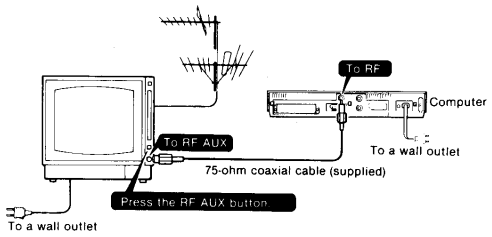
2. Connect a TV receiver to the computer.



Notes

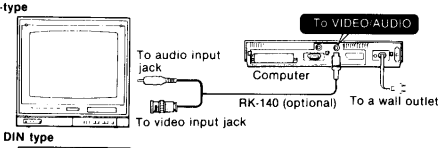
- Set the switch of the antenna selector to the COMPUTER position when using the computer; To watch TV, set it to the AERIAL position.
- Select the channel UHF 36 for the computer.

Connecting a monitor TV with RF AUX connector in front

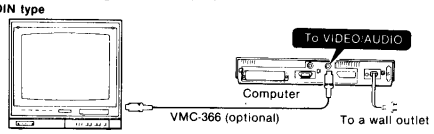


If your monitor TV has an composite video signal input (BNC-type or 6-pin DIN type)

BNC-type

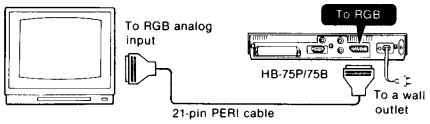


6-pin DIN type

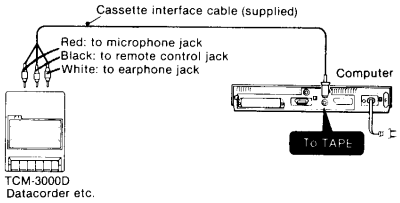


Connecting a color monitor

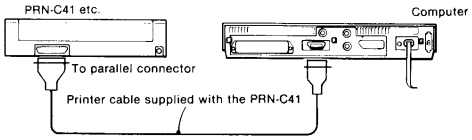
Connect a color monitor having a 21-pin analog RGB signal input.



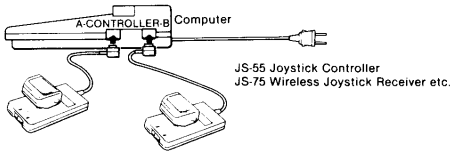
CONNECTING A TAPE RECORDER AS AN EXTERNAL MEMORY



CONNECTING A PRINTER



CONNECTING A JOYSTICK CONTROLLER

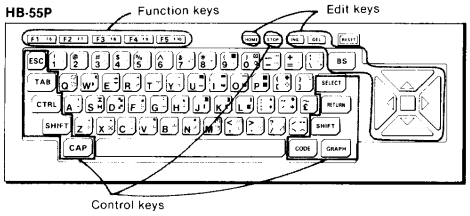


1-5. KEYBOARD OPERATION

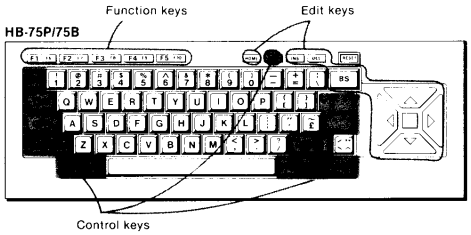
KEY ARRANGEMENT

Alphanumeric characters are arranged in the standard QWERTY typewriter keyboard, as shown below.

HB-55P

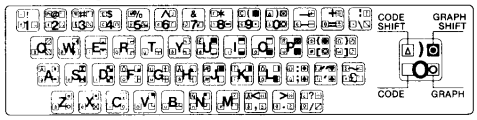


HB-75P/75B



In the HB-55P, the graphic patterns are printed on the keyboard, while in the HB-75P/75B, graphic pattern decal can be affixed to the keyboard.

The supplied graphic pattern sheet is as follows:



To enter these patterns or characters.

The keyboard has character input, control, edit and function keys. When a character input key is pressed, the corresponding character is entered into the computer. When a control key is pressed, the corresponding operation is performed.

Character input keys: A to Z, 0 to 9, +, ?, −, ", and so forth.
The space bar generates a blank space.

Edit keys: HOME, INS, DEL, BS and cursor move keys

Control keys: SHIFT, CAP, CODE, GRAPH, CTRL, TAB, RETURN, ESC, STOP, and SELECT.

Function keys: F1 (F6) to F5 (F10)

CHARACTER INPUT

To enter characters

When a character input key is pressed, the small letter or symbol printed on the lower part on the key top is entered.

Pressed key	Character or symbol to be entered	
T	t	(HB-55P)
6	6	(HB-75P/75B)

When a character input key is pressed with the SHIFT key, the capital letter or symbol printed on the upper part of the key top is entered.

Pressed key	Character or symbol to be entered	
SHIFT + S	S	(HB-55P)
SHIFT + ;	+	(HB-75P/75B)

To enter only capital letters

Depress the CAP key. When this key is pressed, it will lock; when pressed again, it will unlock. While this key locks, the CAP indicator lights up, and the 26 alphabet letters are entered in caps (just as when the SHIFT key is pressed in the normal mode), but numbers and symbols are entered in the normal mode.

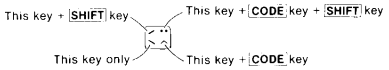
Locked key	Pressed key	Character or symbol to be entered	
CAP	K	K	(HB-55P)
CAP	7	7	(HB-75P/75B)

To put an accent mark on a character

Key is used to put an accent mark on a character.

To put the accent mark printed on the lower-left of the key (`) on a character, first, press key (in this step, no symbol is displayed on the screen). Then, press the character input key needing an accent mark. The character with an accent mark is displayed.

In the same way, to put the accent mark on the upper-left of the key (´), press the key while pressing the SHIFT key. To put the accent mark on the lower-right of the key (^), press the key together with the CODE key. To put the accent mark on the upper-right of the key (¨), press the key while pressing the SHIFT key and the CODE key.



To enter a character or symbol printed on the graphic pattern sheet

The procedure to enter a character or symbol printed on the supplied graphic pattern sheet is as follows:

To enter graphic patterns

To enter the graphic pattern printed on the lower-right part of the key on the graphic pattern sheet, press the corresponding keyboard character input key while pressing the GRAPH key.

Pressed key	Graphic pattern to be entered	
GRAPH + ;	♣	(HB-55P)
GRAPH + Q	▨	(HB-75P/75B)

To enter the graphic pattern printed on the upper-right part of the key on the graphic pattern sheet, press the corresponding keyboard character input key while pressing the GRAPH key and the SHIFT key.

Pressed key	Graphic pattern to be entered	
GRAPH + SHIFT + ;	♫	(HB-55P)
GRAPH + SHIFT + ;	÷	(HB-75P/75B)

To enter special characters

To enter the character or symbol printed on the lower-left part of the key on the graphic pattern sheet, press the corresponding keyboard character input key while pressing the CODE key.

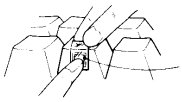
Pressed key	Character or symbol to be entered	
CODE + ;	ø	(HB-55P)
CODE + D	ï	(HB-75P/75B)

To enter the character or symbol printed on the upper-left part of the key on the graphic pattern sheet, press the corresponding keyboard character input key while pressing the CODE key and the SHIFT key.

Pressed key	Character or symbol to be entered	
CODE + SHIFT + 5	¥	(HB-55P)
CODE + SHIFT + N	Ñ	(HB-75P/75B)

Notes

- When using the CODE key, release the CAP lock state.
- In the HB-75P/75B, graphic pattern decal, which can be affixed to the keyboard, is supplied.



Align the line on the decal with the end of the key.
Putting your finger on the pattern, remove the upper decal.

EDIT KEY FUNCTIONS

Keys HOME, INS, DEL, BS and cursor move keys are mainly used for editing a line or screen. Each function is determined by the software used, so read the relevant Software Guide for details.
Under MSX-BASIC, the edit keys function as follows:

HOME key
When this key is pressed, the cursor moves to the upper-left corner of the display screen. The characters displayed on the screen remain.
When pressing this key together with the SHIFT key, the cursor moves to the upper-left corner of the screen, while any character displayed on the screen is erased.

INS (insert) key
Once this key is pressed, the computer is set to the insert mode. In this mode, the cursor becomes smaller and the character at the cursor position and the followings are moved one space to the right when a key is pressed, and you can insert as many characters as you want.
When pressing this key again or moving the cursor with cursor move keys, the insert mode will be released.

DEL (delete) key
The character at the cursor position is deleted. All characters after the deleted character are moved one space to the left.

BS (back space) key
When this key is pressed, the cursor moves one space to the left and the character in that position is deleted.

(cursor move) keys
These keys are used to move the cursor one space in the direction of the triangle: to the right, to the left, up or down. Any character which the cursor moves over does not change.

CONTROL KEY FUNCTIONS

SHIFT key
When this key is pressed together with a character input key, the corresponding symbol in the shift position (upper-left symbol on the key) or corresponding capital letter is entered.

CAP key
When this key is pressed, it will lock so that all letters are entered in capitals. Numbers and symbols will be entered normally even if this key locks. When the key is pressed again, it will unlock. While this key is locked, the CAP indicator lights up.

CODE key
When this key is pressed together with a character input key, the lower-left character or symbol printed on the graphic pattern sheet (supplied) is entered.
When this key is pressed together with a character input key and the SHIFT key, the upper-left character or symbol on the graphic pattern sheet is entered.

GRAPH key
When this key is pressed together with a character input key, the lower-right graphic pattern printed on the graphic pattern sheet is entered.
When this key is pressed together with a character input key and the SHIFT key, the upper-right graphic pattern printed on the graphic pattern sheet is entered.
In the HB-55P, graphic patterns are also printed on the keyboard.

CTRL (control) key
When this key is pressed together with certain keys, a special operation is performed. The key function is determined by the software used. Under MSX-BASIC, the following key combinations are available:

CTRL + B : moves the cursor to the beginning of the word at the cursor position. When the cursor is positioned at the beginning of a word, the cursor moves to the begining of the preceding word.
CTRL + C : releases to input wait state or automatic line number generation.
CTRL + E : deletes the character between the cursor position and the end of the line.
CTRL + F : moves the cursor to the beginning of the next word.
CTRL + G : generates a beep sound.
CTRL + H : has the same function as the BS key.
CTRL + I : has the same function as the TAB key.
CTRL + J : moves the cursor one line down.
CTRL + K : has the same function as the HOME key.
CTRL + L : has the same function as the SHIFT key + HOME key.
CTRL + M : has the same function as the RETURN key.
CTRL + N : moves the cursor to a position next to the last character in the line.
CTRL + R : has the same function as the INS key.
CTRL + U : deletes the characters of the line at the cursor position.
CTRL + X : has the same function as the SELECT key.
CTRL + \ : moves the cursor to the right.
CTRL +] : moves the cursor to the left.
CTRL + ^ : moves the cursor up.
CTRL + _ (underline): moves the cursor down.

TAB key
This key is used to move the cursor to the next tab position. In MSX-BASIC, tabs are set at every eight characters. Any characters which the cursor goes over are deleted when the cursor moves to the next tab position.

RETURN key
Press this key to indicate the end of a line of data or commands input from the keyboard. Press this key every time you finish entering a line.

ESC (escape) key
The function of this key is determined by the software used. Under MSX-BASIC, this key is inoperative.

STOP key
Press this key to interrupt program execution or listing. You can restart the program by pressing this key again.
Pressing this key together with the CTRL key does the same. In this case, however, you can restart program execution with the CONT command, but listing cannot be continued.

SELECT key
The function of this key is determined by the software used. Under MSX-BASIC, this key is not used.

FUNCTION KEYS

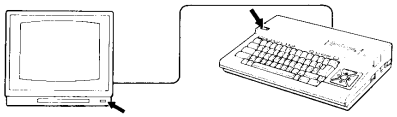
Keys F1 to F5 (F6 to F10) are called function keys. The functions of these keys are determined by the software. Therefore, read the relevant Software Guide for their functions. In MSX-BASIC, keys F1 to F5 function as follows (When these key are pressed while pressing the SHIFT key, they function as keys F6 to F10.):

Function key only	Function key + SHIFT key
F1 color	F6 color 15, 4, 4 RETURN
F2 auto	F7 cload"
F3 goto	F8 cont RETURN
F4 list	F9 list. RETURN
F5 run	F10 cls: run RETURN

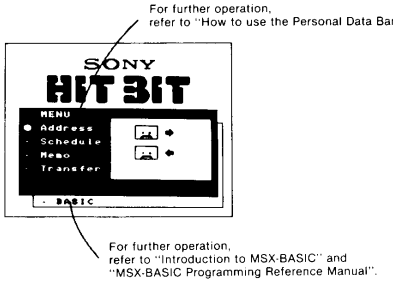
1-6. HOW TO START UP

TO START UP THE PERSONAL DATA BANK OR MSX-BASIC

1. Turn on the monitor TV and the computer.



2. Move the mark ◆ to the desired program of the Personal Data Bank or MSX-BASIC to be executed by using the cursor move keys. Then press the RETURN key.



TO START UP A GAME

Insert the game cartridge into cartridge slot A with the illustration side toward you, or into the cartridge slot B with the illustration side up. Then turn on the monitor TV and the computer.
For details, refer to the game instruction manual.

Note
To power on the computer again, wait more than 10 seconds after it is turned off.

1-7. TO SAVE AND LOAD A MSX-BASIC PROGRAM

The MSX-BASIC program or data entered from the keyboard can be saved on a cassette tape, a data cartridge or a micro floppydisk. This chapter explains how to save a program on a cassette tape and load it from the tape. As to save or load the program using a data cartridge, refer to the instruction manual of the Sony HBI-55 Data Cartridge.

TO SAVE A PROGRAM

1. Insert a cassette tape into the cassette tape recorder, and adjust the volume and tone control to a center position.

2. Type the save command of MSX-BASIC from the keyboard.
   CSAVE "program name"
   Define the program name within six characters. The first character must be a letter.

3. Press the REC (record)/SAVE button of the recorder.
   The tape starts as soon as the button is pressed.

4. Press the RETURN key of the computer.
   The program is then saved on the tape.

5. When a program has been saved and message "OK" is displayed on the screen, press the STOP button of the recorder.

Note
When the remote control plug is connected to the recorder, the tape start and stop functions of the recorder are controlled from the computer.

TO LOAD A PROGRAM

1. Insert the cassette tape containing the desired program into the cassette tape recorder and rewind the tape. Then adjust the volume and tone controls to an appropriate position.

2. Type the load command of MSX-BASIC from the keyboard.
   CLOAD "program name"

3. Press the RETURN key of the computer.

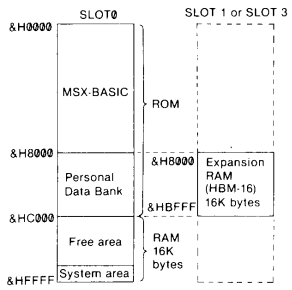
4. Press the PLAY/LOAD button of the recorder.

5. When loading is finished, press the STOP button of the recorder.

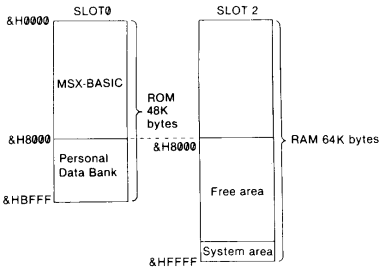
Note
If the program is not loaded, readjust the volume and tone controls and try again.

1-8. MEMORY MAP

HB-55P



HB-75P/75B



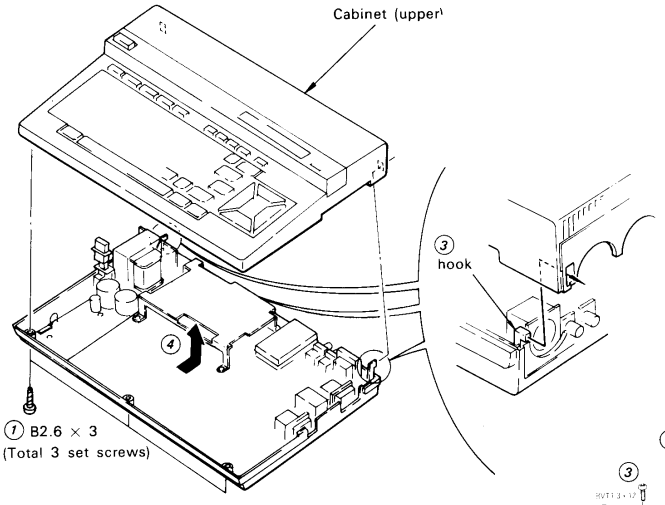
The capacity of the free area can be checked by the FRE function.

CHAPTER 2
SERVICE INFORMATION

2-1. DISASSEMBLY

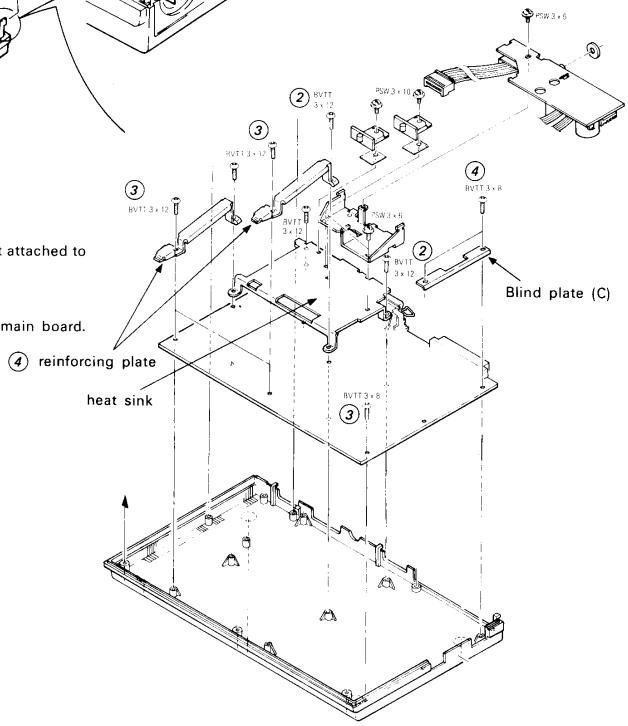
2-1-1. Disassembly of Cabinet (upper)

① Remove the three set screws of cabinet (lower).
② Dis connect the connector CN11 (13P), CN12 (9P) on the main board and CN2 (2P) on the power board.
③ Take off the three hooks.
④ Remove the cabinet (upper) in the direction indicated by the arrow.



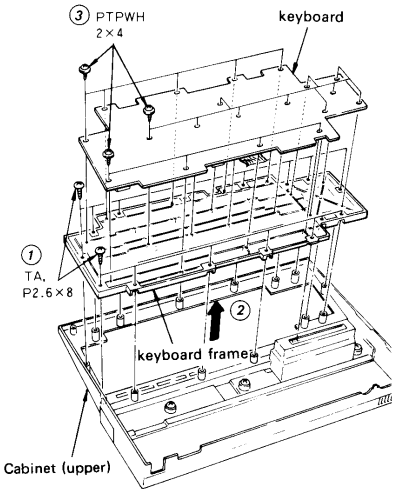
2-1-2. Disassembly of MAIN Board

① Remove the four set screws of heat sink.
Note: The reinforcement (with cushion) is not attached to HB-55P.
② Remove the three set screws of main board.
③ Remove the two set screws of plate (blind).
④ Disconnect the connector CN10 (8P) on the main board.



2-1-3. Disassembly of Keyboard

CAUTION
- HB-55P All the keytops are not locked, therefore remove the keyboard temporarily and taping it.
- HB-75P/75B The function key and cursor key are not locked, therefore remove the keyboard temporarily and taping it.



2-2. PROVIDING OF BASIC ROM AND FIRMWARE ROM

2-2-1. Basic ROM (IC42, 43)

Basic ROM (IC42 and IC43) provides one MASK ROM (MSM38256-70RS). To mount it to IC42, and switch JW5, JW7 to JW10 of MASK/EP switching jumpers to MASK ROM side. (remove IC43)

2-2-2. Firmware ROM (IC44)

Firmware ROM (IC44) provides MASK ROM (MSM38128A-77RS). Remove the jumper JW6 for EP ROM.

2-3. REPAIR PARTS

1. Safety Related Components Warning.
   Components identified by shading marked with ⚠ on the schematic diagrams, exploded views and electrical spare parts list are critical to safe operation. Replace these components with Sony parts whose part numbers appear in this manual or in service bulletins and service manual supplements published by Sony.
2. Replacement Parts supplied from Sony Parts Center will sometimes have a different shape from the original parts. This is due to "accommodating the improved parts and/or engineering changes" or "standardization of genuine parts".
   This manual's exploded views and electrical spare parts list indicate the parts numbers of "the standardized genuine parts at present".
   Regarding engineering part changes in our engineering department, refer to Sony service bulletins and service manual supplements.
3. Printed Components in Bold-Face type on the exploded views and electrical spare parts list are normally stocked for replacement purposes. The remaining parts are not normally required for routine service work. Orders for parts not shown in Bold-Face type will be processed, but allow for additional delivery time.
4. Abbreviations

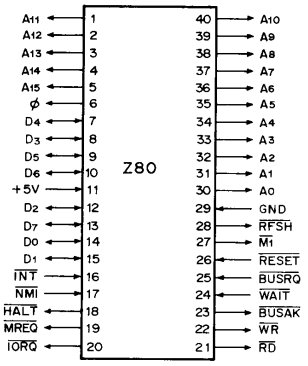
Ref. No.	Description
C□□, CV□□	CAPACITOR
CN□□	CONNECTOR
CP□□	COMBINATION PARTS
D□□	DIODE
DL□□	DELAY LINE
F□□	FUSE
FL□□	FILTER
H□□	HEAD
IC□□	IC
L□□, LV□□	INDUCTOR
M□□	MOTOR
ME□□	METER
PL□□	LAMP
PM□□	SOLENOID
Q□□	TRANSISTOR
R□□, RV□□	RESISTOR
RY□□	RELAY
S□□	SWITCH
SB□□	SOLAR BATTERY
T□□	TRANSFORMER
TH□□	THERMISTOR
X□□	CRYSTAL

5. Units for Capacitors, Inductors and Resistors
   The following units are assumed in schematic diagrams, electrical parts list and exploded views unless otherwise specified:
   Capacitors: μF
   Inductors: μH
   Resistors: ohm

CHAPTER 3
THEORY OF OPERATION

3-1. Z80 (CPU)

The Z80 has 40 pins, and they are arranged as follows:



3-1-1. Functions of Pins

① **A0 to A15 (Address bus)**
A bus line which outputs addresses when reading and writing of the memories and input/output operations.

② **D0 to D7 (Data bus)**
A bus line which reads and outputs the data.

③ **MREQ and IORQ**
MREQ is output when accessing to memory, and IORQ is output when accessing to I/O port. The I/O port is an address for controlling the printer and PSG.

④ **RFSH**
Dynamic RAM (for example 4116) is not able to memorize unless it is refreshed at certain time intervals. RFSH is the timing signal for this refreshing purpose.

⑤ **M1**
It indicates a cycle in which the CPU reads out a command to the exterior.

⑥ **HALT**
It is signal which informs the outside that the HALT (STOP) command has been executed and that CPU has ceased the carrying out of the program. This HALT will continue until it is interrupted or reset.

⑦ **WAIT**
This is a signal which awaits the CPU processing until the peripheral device has completed its operation, since the peripheral device cannot catch up with the processing speed of the CPU.

⑧ **INT and NMI**
They are input pins for interruptions.
NMI enables interruption at any time.
INT enables prohibition of interruption in accordance with contents of a program.

⑨ **RESET**
A pin which initializes the CPU.

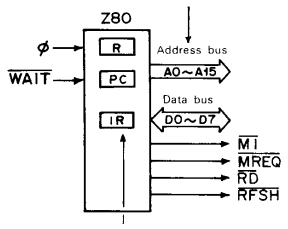
⑩ **BUSRQ and BUSAK**
BUSRQ is a pin which requests the CPU to disconnect addresses and data buses from the CPU.
BUSAK is a pin which informs the exterior that the CPU accepts the BUSRQ.

⑪ **RD and WR**
WR signal is output when writing is performed for the memory or I/O devices.
RD signal is output when reading is performed for the memory or I/O devices.

3-1-2. Operation of Z80

When power supply of the Z80 is turned ON, RESET signal is fed to it to clear out its internal memory contents.
The RESET pin of the Z80 becomes active when set at "L". Therefore, when "L" signal is applied to it, the pins of the Z80 are established as follows:
[Address and data bus]
Both become "H" level. (Floating condition)
[Control pins]
All the control pins output non-active signals.
The signal level of these pins when the Z80 is in active mode is "L" level; therefore, in this state, the Z80 outputs "H" level.
[Program counter]
The contents of the program counter become 0000H.
[Interruption enabling flip-flop]
Becomes zero and becomes prohibition of interruption.
[Interruption mode]
The interruption mode becomes zero.
[Interruption page address register]
The contents of I register become 00H.
[Refresh register]
The contents of R register become 00H.
[Register file]
The contents of all registers such as A, B, C, D, E, F, A', B', C', D', E', F', IX, IY, H, L, and R become 00H.
When RESET becomes "H" from "L", the Z80 starts to execute operation of the program; however, the contents of the program counter (PC) become command fetch address. This means that the operation code comes from the 0000H address. The Z80 fetches the operation codes when it internally becomes into "a condition to execute operation fetch codes".

At first, the contents of the program counter (PC) are output, and then the contents of the refresh register (R) are output after the Z80 fetches the operation code.



From the address of the memory, which is specified by the program counter, a part of the operation code is fetched to the command register (IR).

3-1-3. M1 Cycle

A sequence to fetch an operation code is called M1 cycle.

① When the Z80 becomes M1 cycle.

② During the interval between the arrivals of the first clock signal and the second clock signal (it is called T_1 state), the contents of the program counter are output to the address bus.

③ When it is also in the T_1 state, "L" is output to $\overline{M1}$. At this time, the Z80 is operating in M1 cycle, and it plays a role to inform the outside that an address to fetch the operation code on the address bus is being output.

④ When it is also in the T_1 state, "L" is output to $\overline{MREQ}$ and $\overline{RD}$.
Access the memory with these signals and fetch the operation code (to the command register).

⑤ When it is in T_2 state, if an external input to $\overline{WAIT}$ pin of the Z80 is "H", the Z80 moves to T_3 state. If the $\overline{WAIT}$ pin is in "L" level, the Z80 does not move to T_3, but it becomes in wait state (TW), and waits until it becomes "H".

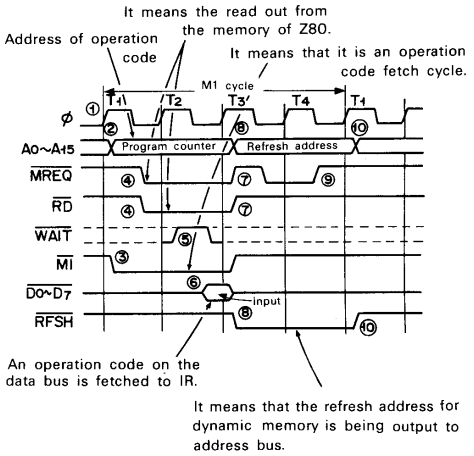
⑥ At a point when the Z80 moves to T_3 state from T_2 state, it fetches the operation code, which is read out on data bus (D_7 to D_0) from the memory, to the command register (when the clock of T_3 is being raised up).

⑦ In T_3 state, $\overline{MREQ}$ becomes at first "H" and then returns to "L" again.

⑧ In T3 state, the contents of the refresh register are output to the address bus. However, among the 8 bits of the refresh register, the lower 7 bits are output to the lower 7 bits of the address bus.
To indicate that the refresh address is being output to the address bus, "L" is output to $\overline{RFSH}$ pin.

⑨ When the Z80 becomes in T_4 state, the $\overline{MREQ}$ signal returns to "H" from "L".
It becomes possible to refresh the dynamic memory with the $\overline{MREQ}$, $\overline{RFSH}$ and the address bus.

⑩ In the following Fig., up to the T_4 state shows an operation code fetch cycle. The place marked 10 denotes the T_1 state in a cycle whichever comes next. (It depends on the command fetched immediately before.)
Up to this point, the refresh address has been output to the address bus, and $\overline{RFSH}$ signal which indicates the above-mentioned state has been set at "L". However, the $\overline{RFSH}$ signal also becomes "H" simultaneously when the refresh address on the address bus disappears.



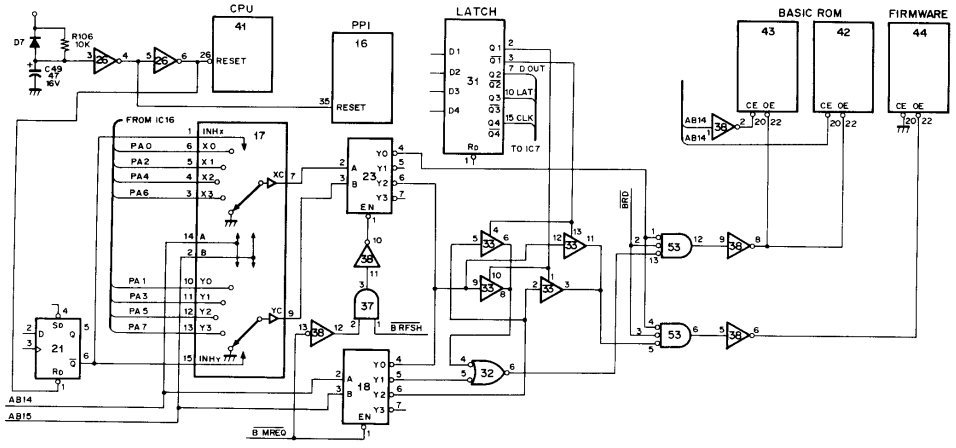
Command OP code fetch cycle (M1 cycle)

3-1-4. Refresh Cycle

Refresh cycle is an indispensable and troublesome operation for DRAM. The memorized contents of the memory will be erased unless the specified row address is not accessed within the determined length of time. The term of row address access used here means that only row address and $\overline{RAS}$ are necessary. Accordingly, even in a normal read cycle and a write cycle, refresh has been completed against their row addresses.
The Z80 CPU outputs address in T_1 and T_2 of the OP code fetch cycle and indicates the output to the memory, and it fetches OP code at the clock rising up of T_3, and performs refresh of the dynamic memory at the rest of 2 states (T_3 and T_4).
There are two methods of refreshing. The first method is to refresh the 128 row addresses continuously (Burst mode refreshing) and the other is a dispersing method to refresh each row within 2ms (Single mode refreshing).
The Z80 is so designed as to be refreshed by conveniently using the latter method.
For the Z80, refreshment is performed so that a row address is refreshed once every M1 cycle. During the refreshing operation, $\overline{CAS}$ output is kept at H level.
Simultaneous refreshing is possible even if the data outputs of several memories are connected with the wired OR. The refreshing operation is a quasi read operation, and data in the memory is not output at that time.
The refreshing operation using only $\overline{RAS}$ is called $\overline{RAS}$ only refreshment. Driving of refreshing cycle of the dynamic memory can be performed by the $\overline{RFSH}$ and $\overline{MREQ}$ signals.

3-2. OPERATION WHEN POWER SUPPLY IS TURNED ON

When the power supply is turned ON, "L" signal is applied to pin 3 of IC26 during several hundreds msec with a time constant of R106 and C49. This "L" signal is inverted to "H", and applied to pin 35 ($\overline{RESET}$) of IC16 (PPI). Furthermore, this "H" signal is inverted to "L" signal, and it is applied to pin 26 ($\overline{RESET}$) of IC41 (CPU). (IC26 is an inverter of the Schmitt trigger type.)
When resetting signal is applied to IC41 (CPU), the CPU turns all of its controlling pins and address data buses to "H" levels.
Pin 6 of IC21 is at "H" level. Pin 6 becomes "H" level, since "L" level is applied to pin 1 of IC21 with $\overline{RESET}$ signal.
IC16 (PPI) is initially set, and this condition contunues until something is written into A port. When pin 6 of IC21 turns to "H", it turns pins 1 and 15 of IC17 to "H". When pins 1 and 15 of IC17 become "H", pins 7 and 9 both become "L".
When pin 26 of IC41 turns to "H" from "L", this releases the resetting of the CPU, and it outputs 0000_H into the address bus and turns $\overline{MREQ}$ signal to "L". Furthermore, pin 2 of IC37 turns to "H" with the inverter of IC38.
$\overline{RFSH}$ signal ("H") is applied to pin 1 of IC37. The output of "H" of IC37 is inverted with IC38 and "L" signal is applied to pin 1 of IC23. This turns pin 4 to "L". This "L" signal is applied to pins 1 and 4 of IC53.
On the other hand, $\overline{MREQ}$ signal and signals of the address bus AB14 and 15 are applied to pins 1, 2 and 3 of IC18, respectively.
Pin 4 becomes "L", as "L" level signal is applied to pins 2 and 3 of IC18.
Owing to this, pins 9 and 12 of IC33 become "L". However, pin 2 of IC31 is set at "L" and pin 3 of IC31 is set at "H" by the RESET signal "H", and "L" level of pin 12 of IC33 turns pin 5 of IC53 to "L". By turning $\overline{BRD}$ signal to "L", pins 3, 4, and 5 of IC53 are all turned to "L".
Consequently, pin 22 of IC44 becomes "L", and a program stored in MASK ROM of FIRMWARE starts to run. (At this point, BASIC has not started yet.)
This program is a PLL Setting Data Sending Out Program which sends the data to IC31. Signals are fed from pins 7, 10, and 15 of IC31 to pins 2, 3, and 4 of IC7, and then the PLL starts to operate. Subcarrier of 4.43MHz of PAL signal is oscillated.
After that pin 3 of IC31 is set at "L" and pin 2 is set at "H". Accordingly, pin 8 of IC33 becomes "L", and pin 4 of IC32 also becomes "L", and output of pin 6 becomes "L". Pins 1, 2, and 13 of IC53 become "L", and pins 22 of IC42 and IC43, also become "L" IC42 (BASIC ROM) is selected and is entered into BASIC program.
Pin 20 ($\overline{CE}$) of IC42 is connected to AB_{14} of the address bus. When AB_{14} becomes "H", ROM of IC42 is unable to be selected. (IC42 has a capacity of 16K bytes from 0000_H to $3FFF_H$.)
Since AB_{14} is inverted and connected to pin 20 ($\overline{CE}$) of IC43, when AB_{14} becomes "H", pin 20 ($\overline{CE}$) of IC43 becomes "L".
At the same time, AB_{14} and AB_{15} of the address bus are connected to the inputs of pins 2 and 3 of IC18, and because AB_{14} is at "H" and AB_{15} is at "L", output of pin 5 becomes "L" and pin 6 of IC32 becomes "L". This causes pin 22 ($\overline{OE}$) of IC43 to become "L" through IC53 and IC38, and to select ROM of IC43.
(IC43 has a capacity of 16K bytes from 4000_H to $7FFF_H$.) When address becomes 8000_H next to $7FFF_H$, AB_{15} becomes "H" and AB_{14} becomes "L".
This address data is applied to IC17 and IC18, and the contents of pins 4 (X_2), and 12 (Y_2) are output to pins 7 (XC) and 9 (YC). However, as they have all become "L", thus the output of pin 4 of IC23 becomes "L".
This signal is applied to pins 1 and 4 of IC53.
On the other hand, as address data AB_{15} ("H") and AB_{14} ("L") are applied to pins 2 and 3 of IC18, output of pin 6 becomes "L" and outputs of others become "H". As pins 4 and 5 of IC18 become "H", "H" is output to pin 6 of IC32.
Accordingly, "H" is applied to pin 13 of IC53, so that pin 12 of IC53 becomes "L" and output of pin 9 of IC38 becomes "H", and ROMs of IC42 and IC43 cannot be selected. On the other hand, output "L" of pin 6 of IC18 is input to pin 2 of IC33 and "L" is output to pin 3 (pin 1 of GATE is at "H"). Then pins 3, 4, and 5 of IC53 all become "L", and output "H" of pin 6 of IC53 is inverted with IC38, and thus pin 6 of IC38 becomes "L".
The pin 6 of IC38 is connected to pin 22 ($\overline{OE}$) of IC44 and it selects IC44 (FIRMWARE ROM). The ROM of IC44 is continuously selected until pin 6 of IC53 becomes "L" (9000_H).
Accordingly, IC44 is capable of using 8000_H to $8FFF_H$.



3-3. CHECKING SLOT

When the MSX-BASIC program starts operation, it executes initial setting and then checks the slot. The checking is performed in sequential order beginning with slot 0.
In this system, slot 0 is the memory stored within this system, and slot 1 is the upper cartridge slot and slot 3 is the rear cartridge slot.
In the HB-75, MAIN RAM 64K is assigned to slot 2.
When IC44 is selected, the program of IC44 is performed. During the performance of this program, check to see what kind of items are inserted into this cartridge slot. At this time, if instantaneously executable ROMs such as game cartridge are inserted, execution of controlling is shifted to them.
Selection of the slots is performed with IC23. IC23 is controlled with data from the PPI(IC16).
When pin 4 of IC23 is "L", slot 0 is selected.
When pin 5 of IC23 is "L", slot 1 is selected.
When pin 6 of IC23 is "L", slot 2 is selected.
When pin 7 of IC23 is "L", slot 3 is selected.
Selection of the memories is performed with IC18, and it works as follows:
When pins 4 and 5 of IC18 are "L" (addresses 0000_H to $7FFF_H$), MSX-BASIC ROMs of IC42 and IC43 are selected.
When pin 6 is "L" (addresses 8000_H to $8FFF_H$), IC44 is selected.
When pin 7 of IC18 is "L" (address over $C000_H$), MAIN RAM is selected. (HB-55P).

IC23 (2/2) selects ROM of the cartridge slot.
IC23 (2/2) operates only when the $\overline{MREQ}$ and $\overline{RD}$ are "L", and selects ROM of the cartridge slot.
Interchange of data between cartridge slots and external I/O is carried out through IC40, and IC40 is controlled by IC52, IC37, and IC38.
When pin 19 of IC40 is "H", it becomes in the OFF state, and interchange of data is accordingly not carried out. When the CPU is accessed to PPI, PSG, and VDP, it turns pin 19 to "H" and closes the gate. The circuit diagram at that time is as shown in Fig. 1.

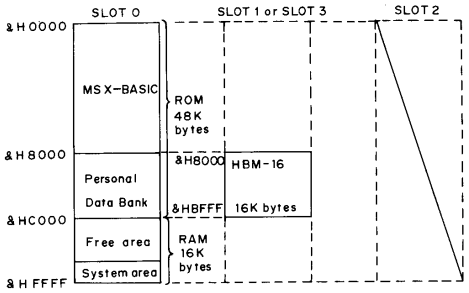
- When pin 19 of IC40 becomes "H":
  1. When the $\overline{IORQ}$ signal is at "L" level, and either one of PPI, PSG, and VDP is at "L" level.
  2. When either one of the $\overline{M1}$ signal or $\overline{IORQ}$ signal is at "H" level.
  3. When the slot 0 is selected. (The ICs 29 and 30 are so designed as to input "L" level always to pin 10 of IC27 when addresses are 0000_H to FFF_H.)

  When one of the conditions is applicable to the above-mentioned 1 to 3, the data coming through IC39 are not carried out.
- When pin 19 of IC40 becomes "L", interchange of data is carried out, and the direction of the inerchange of data is determined by pin 1 .
  When pin 19 becomes "L":
  1. Any slot except slot 0 is selected.
  2. When access is not performed to the internal I/O device (PPI, PSG and VDP).

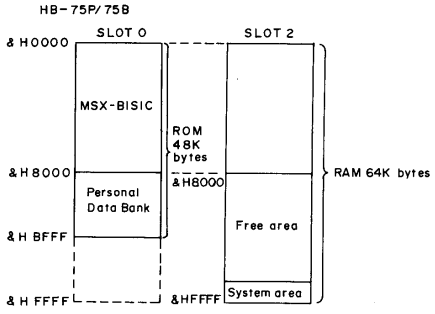
  When the above-mentioned two conditions are coincided.
- When pin 19 is at "L" level and pin 1 is at "H" level, data are sent out from interior of the system.
  When pin 1 is at "L" level:
  When $\overline{RD}$ is at "L" level, or $\overline{M1}$ and $\overline{IORQ}$ are simultaneously at "L" level. Except for the above, they are all "H" level.
  When pin 1 is at "L" level, data are read into the system from the exterior.

MEMORY MAP

HB-55P



HB-75P/75B



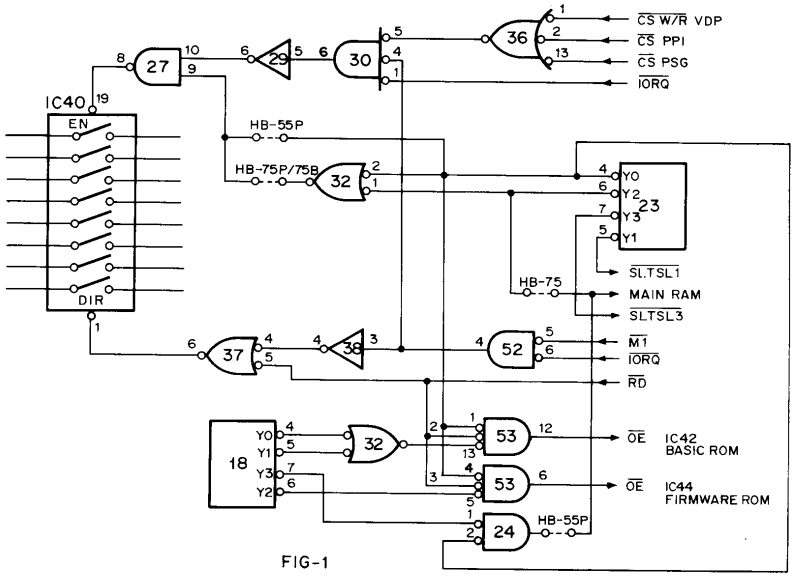


FIG-1

Each pin of the cartridge slot

Pin No.	Name	Content
1	$\overline{CS1}$	Address selecting signal of memory 4000H to 7FFFH
2	$\overline{CS2}$	Address selecting signal of memory 8000H to BFFFH
3	$\overline{CS12}$	Address selecting signal of memory 4000H to BFFFH (for 256K ROM)
4	$\overline{SLTSL}$	It is a slot selecting signal, which applies selecting signals peculiar to each of the respective slots.
5	Spare	Spare signal line for future use (Prohibited to be used)
6	$\overline{RFSH}$	Refreshing cycle signal
7	$\overline{WAIT}$	WAIT request signal for CPU (Timing should be taken at the interior of the system.)
8	$\overline{INT}$	Interruption request signal for CPU
9	$\overline{M1}$	Indicating signal of fetch cycle of CPU
10	$\overline{BUSDIR}$	Direction control signal of external data bus buffer
11	$\overline{IORQ}$	Request signal of I/O
12	$\overline{MREQ}$	Request signal of memory
13	$\overline{WR}$	Write timing signal
14	$\overline{RD}$	Read timing signal
15	$\overline{RESET}$	System reset signal
16	Spare	Spare signal line for future use (Prohibited to be used)
17 to 32	A0 to A15	Address bus signal
33 to 40	D0 to D7	Data bus signal
41 and 43	GND	Ground
42	CLOCK	CPU CLOCK (3.579545MHz)
44 and 46	SW1 and SW2	Protection for plugging in and out
45 and 47	+5V	Power supply of +5V
48	+12V	Power supply of +12V
49	SUNDIN	Sound input signal (−5 dBm)
50	−12V	Power supply of −12V

3-4. I/O PORT

For selecting of I/O port, address decoder of IC23 is used. The following operations are performed in order that the CPU accesses to the I/O port.

3-4-1. Selection of I/O Port

When reading out

① Number of input port is output to the address bus.
② When it is in T_2 state, "L" is output to $\overline{IORQ}$ and $\overline{RD}$. This means to access input port.
③ When $\overline{WAIT}$ is either "L" or "H", the Z80 moves automatically to Tw.
④ If in TW state, if the input to $\overline{WAIT}$ is at "H" level, the Z80 extricates itself from the Tw state and shifts into T_3 state.
⑤ The data which are read out from the input port on the data bus are read into interior of the Z80.
At this time, the $\overline{IORQ}$ and $\overline{RD}$ return to "H" from "L".

When writing in

①' Number of output port is output to an address.
①" Data to be written onto the output port is output to the data bus.
②' In T_2 state, "L" is output to the $\overline{IORQ}$ and $\overline{WR}$. This means to access output port.
③' Whether the $\overline{WAIT}$ is "L" or "H", the Z80 moves automatically to Tw.
④' In Tw state, if the $\overline{WAIT}$ is "L", the Tw state is continuously inserted; however, if the $\overline{WAIT}$ is "H", the Z80 moves to T_3 state.
⑤' In T_3 state, the $\overline{IORQ}$ and $\overline{WR}$ return to "H" from "L". This means that the data has been written out to the output port.

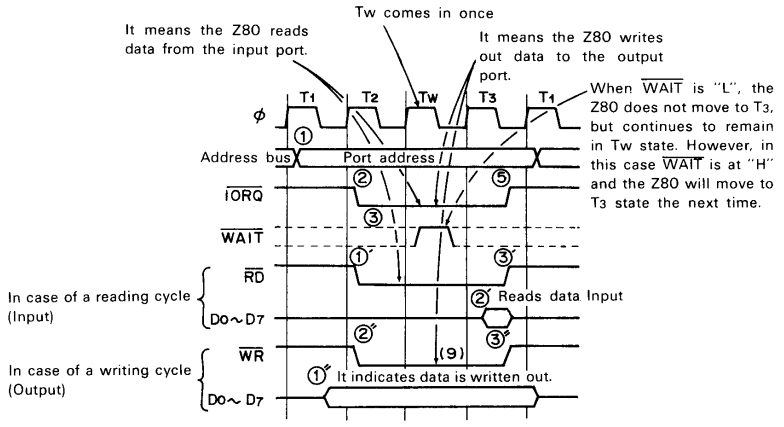
The signal on the address bus of the input and output commands are output to the lower 8 bits of input and output port numbers, and the contents of the accumulator or B register are output to the upper 8 bits of the signal.
A_3 and A_4 of the address bus are applied to input pins 13 and 14 of address decoder of IC23. Furthermore, A_4 to A_7 of the address bus are applied to pin 15 ($\overline{EN}$) through IC25, IC27, IC28, IC29, and IC37. Depending on this signal, it is determined that which I/O device is selected. The selection can be made as follows:

A_7	A_6	A_5	A_4	A_3		I/O port address
1	0	0	1	0	PRINTER	90H, 91H
1	0	0	1	1	VDP	98H, 99H
1	0	1	0	0	PSG	A0H~A3H
1	0	1	0	1	PPI	A8H~ABH

These are all selected when the $\overline{IORQ}$ and $\overline{RD}$ or $\overline{WR}$ signals are output.

3-4-2. Operation of Each Port

PRINTER: It sets data at 91H and outputs data at 90H (strobe pulse and BUSY pulse).
VDP: 99H means time to transfer address, and 98H means time to transfer data.
PSG: A0H Specifies register.
A1H Write data into register.
A2H Contents of register are output to data bus.
A3H Not operated
PPI: When $\overline{RD}$ is "L":
A8H Contents of port A are output to data bus.
A9H Contents of port B are output to data bus.
AAH Contents of port C are output to data bus.
ABH is prohibited.
When $\overline{WR}$ is "L":
A8H Contents of data bus are output to port A.
A9H Contents of data bus are output to port B.
AAH Contents of data bus are output to port C.
ABH Contents of data bus are written into control register.



3-5. ACCESS TO MAIN RAM (HB-55P)

In the HB-55P system, a RAM of 16K bytes is mounted. Access to the is RAM can be carried out when the address data becomes over $C000_H$.

3-5-1. When Data is Read Out from RAM (HB-55P)

Address data is applied to input pins of IC49 and IC57, and at this time, the pins 1 (A) of IC49 and IC57 become "L"; accordingly, the contents of the 0 group are output to the output pins. These form a ROW address. Nextly, when pin 19 ($\overline{MREQ}$) of IC41 (CPU) becomes "L", the signal is applied to pin 12 of IC37. Accordingly, "L" is output to pin 11 of IC37. This signal is applied to pin 2 (D) of IC51. A clock signal is applied to pin 3 of IC51, and with the rising up of this clock signal the contents of pin 2 are output to pin 5 . Owing to this, "L" is applied to each $\overline{RAS}$ pin of the dynamic RAM of IC58 to IC61 and IC65 to IC68.

Consequently, the ROW address is latched into the memory.

$\overline{MREQ}$ signal from IC41 (CPU) is applied to pin 1 of IC18. At this time, since signals of AB_{14} and AB_{15} of the address data are applied to pins 2 and 3 of IC18, all these pins become "H"; accordingly, pin 7 of IC18 becomes "L". This signal is applied to pin 1 of IC24. At this time, pin 2 of IC24 is also "L" and therefore, pin 3 of IC24 becomes "L", and the signal is also applied to pin 12 of IC50.

As IC50 operates in just the same manner as the above-mentioned IC51, pin 9 of IC50 becomes "L". At this time, pin 8 of IC50 becomes "H" and the signal is applied to pins 1 of IC49 and IC57 . Accordingly, contents of 1 group are output to the outputs of IC49 and IC57. (It becomes COLUMN address.)

The signal from pin 9 of IC50 is applied to pin 12 of IC51, and its contents are output to pin 9 of IC50 with the clock signal. It takes 10ns for this process. (10ns delayed).

During this time interval, the address data depending on outputs of IC49 and IC57 becomes stable. The pin 9 of IC51 is connected to pin 15 ($\overline{CAS}$) of the dynamic memory, and by setting it to "L" the COLUMN address is latched into memory.

When $\overline{MREQ}$ signal becomes "H" from "L", pin 2 of IC51 becomes "H" from "L", and pin 5 (Q) also becomes "H". Accordingly, pin 4 ($\overline{RAS}$) of the memory becomes "H" from "L". Pin 6 of IC51 becomes "L" from "H", and this signal is applied to pins 10 ($\overline{PRESET}$) of IC50 and IC51 to shift the output of pin 9 of IC51 to "H".

As a result, pin 15 ($\overline{CAS}$) of the memory becomes "H" and the contents of the previously set address becomes to be read out from the memory.

When $\overline{RFSH}$ signal of "L" level is applied to pin 13 of IC37 from the CPU, pin 11 of IC37 also becomes "L", and the signal is also applied to pin 2 of IC51. Therefore, "L" is output to pin 5 of IC51 and the refreshing of the dynamic memory is carried out.

When pin 13 (signal of $\overline{RFSH}$) and pin 12 (signal of $\overline{MREQ}$) of IC37 all become "H", pin 5 of IC51 becomes "H" and pin 4 ($\overline{RAS}$) of the memory becomes "H".

3-5-2. When Data is Written into RAM (HP-55P)

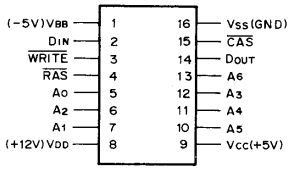
When data is written in, $\overline{MREQ}$ signal and $\overline{WR}$ signal of "L" level are output from the CPU. The process to set an address to the memory is the same as in the data reading out.

Output timing of $\overline{WR}$ signal from the CPU is slightly later than that of $\overline{MREQ}$ signal. Therefore, during this time interval, setting of address is carried out.

$\overline{WR}$ signal is applied to pin 9 of IC24 and $\overline{MREQ}$ signal is applied to pin 10 .

When pins 9 and 10 are "L", pin 8 becomes "L", and shift pin 3 ($\overline{WE}$) of the memory to "L" to write in the data to the address which has previously been set.

3-5-3. Dynamic RAM (4116) (HB-55P)



$A_0 - A_6$	Address input
$\overline{CAS}$	Column address strobe
D_{IN}	Data intput
D_{OUT}	Data output
$\overline{RAS}$	ROW address strobe
$\overline{WRITE}$	Read/write input
V_{BB}	Power supply (−5V)
V_{CC}	Power supply (+5V)
V_{DD}	Power supply (+12V)
V_{SS}	GND

The above shows the pin connection diagram of dynamic RAM (4116).

The memory cells of 16384 (1024×6) are composed of 128 rows×128 columns.

To select each memory cell, 7 bits of ROW address and 7 bits of column address are necessary. However, there are only 7 (A_0 to A_6) address input pins on the memory chip.

As a result, to input 14 bits of an address to the memory chip, input has to be carried out twice, that is by dividing the 14 bits of address into two parts of 7 bits each.

3-5. ACCESS TO MAIN RAM (HB-75P/75B)

In the HB-75P/75B system, a RAM of 64K bytes is mounted. Access to this RAM can be carried out when the slot 2 is selected.

3-5-1. When Data is Read Out from RAM (HB-75P/75B)

Address data is applied to input pins of IC49 and IC57, and at this time, the pins 1 (A) of IC49 and IC57 become "L"; accordingly, the contents of the 0 group are output to the output pins. These form a ROW address. Nextly, when pin 19 ($\overline{MREQ}$) of IC41 (CPU) becomes "L", the signal is applied to pin 12 of IC37. Accordingly, "L" is output to pin 11 of IC37. This signal is applied to pin 2 (D) of IC51. A clock signal is applied to pin 3 of IC51, and with the rising up of this clock signal the contents of pin 2 are output to pin 5. Owing to this, "L" is applied to each $\overline{RAS}$ pin of the dynamic RAM of IC58 to IC61 and IC65 to IC68.

Consequently, the ROW address is latched into the memory.

$\overline{MREQ}$ signal from IC41 (CPU) is applied to pin 1 of IC18. At this time, since signals of AB_{14} and AB_{15} of the address data are applied to pins 2 and 3 of IC18, all these pins become "H"; accordingly, pin 7 of IC18 becomes "L". This signal is applied to pin 1 of IC24. At this time, pin 2 of IC24 is also "L" and therefore, pin 3 of IC24 becomes "L", and the signal is also applied to pin 12 of IC50.

As IC50 operates in just the same manner as the above-mentioned IC51, pin 9 of IC50 becomes "L". At this time, pin 8 of IC50 becomes "H" and the signal is applied to pins 1 of IC49 and IC57. Accordingly, contents of 1 group are output to the outputs of IC49 and IC57. (It becomes COLUMN address.)

The signal from pin 9 of IC50 is applied to pin 12 of IC51, and its contents are output to pin 9 of IC50 with the clock signal. It takes 10ns for this process. (10ns delayed).

During this time interval, the address data depending on outputs of IC49 and IC57 becomes stable. The pin 9 of IC51 is connected to pin 15 ($\overline{CAS}$) of the dynamic memory, and by setting it to "L" the COLUMN address is latched into memory.

When $\overline{MREQ}$ signal becomes "H" from "L", pin 2 of IC51 becomes "H" from "L", and pin 5 (Q) also becomes "H". Accordingly, pin 4 ($\overline{RAS}$) of the memory becomes "H" from "L". Pin 6 of IC51 becomes "L" from "H", and this signal is applied to pins 10 ($\overline{PRESET}$) of IC50 and IC51 to shift the output of pin 9 of IC51 to "H".

As a result, pin 15 ($\overline{CAS}$) of the memory becomes "H" and the contents of the previously set address becomes to be read out from the memory.

When $\overline{RFSH}$ signal of "L" level is applied to pin 13 of IC37 from the CPU, pin 11 of IC37 also becomes "L", and the signal is also applied to pin 2 of IC51. Therefore, "L" is output to pin 5 of IC51 and the refreshing of the dynamic memory is carried out.

When pin 13 (signal of $\overline{RFSH}$) and pin 12 (signal of $\overline{MREQ}$) of IC37 all become "H", pin 5 of IC51 becomes "H" and pin 4 ($\overline{RAS}$) of the memory becomes "H".

3-5-2. When Data is Written into RAM (HP-75P/75B)

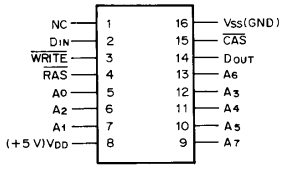
When data is written in, $\overline{MREQ}$ signal and $\overline{WR}$ signal of "L" level are output from the CPU. The process to set an address to the memory is the same as in the data reading out.

Output timing of $\overline{WR}$ signal from the CPU is slightly later than that of $\overline{MREQ}$ signal. Therefore, during this time interval, setting of address is carried out.

$\overline{WR}$ signal is applied to pin 9 of IC24 and $\overline{MREQ}$ signal is applied to pin 10.

When pins 9 and 10 are "L", pin 8 becomes "L", and shift pin 3 ($\overline{WE}$) of the memory to "L" to write in the data to the address which has previously been set.

3-5-3. Dynamic RAM (3764) (HB-75P/75B)



A_0 – A_7	Address input
$\overline{CAS}$	Column address strobe
DIN	Data input
DOUT	Data output
$\overline{RAS}$	ROW address strobe
$\overline{WRITE}$	Read/write input
VDD	Power supply (+5V)
VSS	GND

The above shows the pin connection diagram of dynamic RAM (3764).

The memory cells of 65536 (4096×16) are composed of 512 rows ×512 columns.

To select each memory cell, 8 bits of ROW address and 8 bits of column address are necessary. However, there are only 8 (A0 to A7) address input pins on the memory chip.

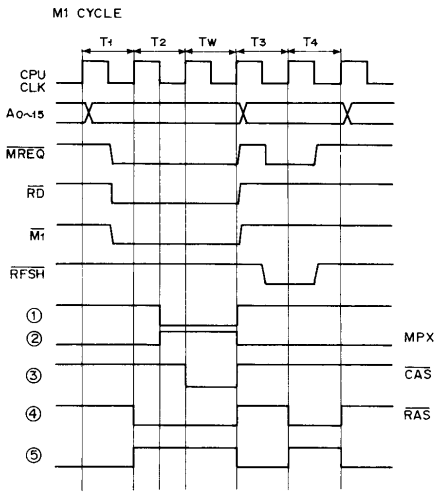
As a result, to input 16 bits of an address to the memory chip, input has to be carried out twice, that is by dividing the 16 bits of address into two parts of 8 bits each.

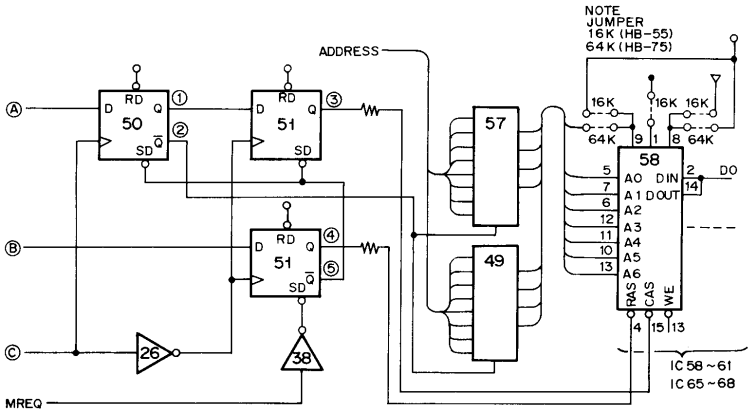
3-5-4. Read Cycle Procedure

(1) Determine the row address.
(2) Drop $\overline{RAS}$. (Internally latch the 7-bit (HB-55)/8-bit (HB-75) row address.)
(3) Determine the column address.
(4) Drop $\overline{CAS}$. (Internally latch the 7-bit (HB-55)/8-bit (HB-75) row address.)
(5) Raise $\overline{RAS}$.
(6) Raise $\overline{CAS}$ after reading data.

The write cycle, excluding $\overline{WRITE}$, is carried out in the same manner as the read cycle.

There are 2 write modes. One is called the early write mode in which $\overline{WRITE}$ falls before $\overline{CAS}$ falls. The other is called the delay write mode in which $\overline{WRITE}$ falls while $\overline{CAS}$ is being low. The read cycle is normally carried out in the early write mode.



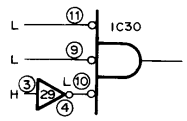


Ⓐ : When the signal in line Ⓐ is set at "L" by Memory Select, a read/write operation can be done for the memory.
Ⓑ : When the signal in line Ⓑ is set at "L" by Memory Select/Refresh, RAS is issued.
Ⓒ : The signal in line Ⓒ indicates the same clock as CPU CLOCK.

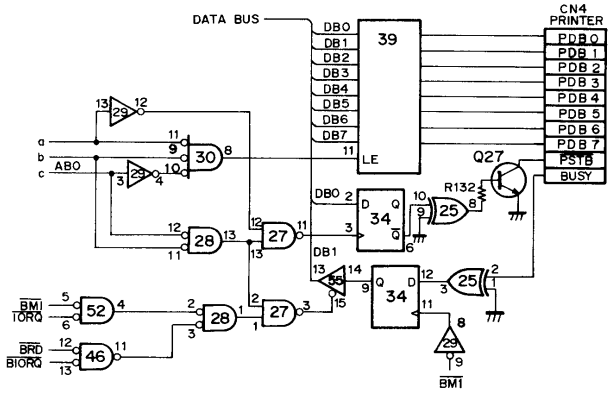
3-6. PRINTER

IC30 is a 3-input NOR gate. When all input signals are "L", the output signal at pin 8 of IC30 is "H". Pin 8 of IC30 is connected to pin 11 of IC39. When the signal at pin 8 of IC30 is "H", data can be IC39.
The following signals are applied to IC30.

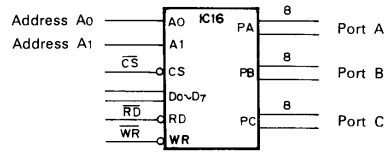
a. When both $\overline{IORQ}$ and $\overline{WR}$ are "L", the signal at pin 11 of IC30 is "L".
b. When pin 9 of IC30 is selected by address decoder, the signal at pin 9 of IC30 becomes "L".
c. When ABO in the address bus is "H", the signal at pin 10 of IC30 is "L".



In the above state, data can be issued on the printer. Thereafter, the printer starts printing data when a strobe signal is issued to the printer.
Select 91H at the I/O port, latch the print data, and send a strobe signal in 90H. Then, control accesses the printer.
The strobe signal is issued in the following manner.
Signals identified by a, b, and c are fed to inverter IC29 and NOR gate IC28.
The I/O port is set in 90H at this time. ABO in the address bus is low and the address decoder (at pin 10 of IC23) selects the printer. Thus, both $\overline{IORQ}$ and $\overline{WR}$ become "L".
The input signals at pins 11 and 12 of IC28 are "L" and the otuput signal at pin 13 of IC28 is "H". The input signal at pin 13 of IC29 is "L" and the output signal at pin 12 of IC29 is "H". The signals at pin 13 of IC28 and pin 12 of IC29 are fed to pins 13 and 12 of IC27, respectively. The signal at pin 11 of IC27 becomes "L" and it is fed to pin 3 of IC34. When either $\overline{IORQ}$ or $\overline{WR}$ becomes "H", the signal at pin 13 of IC29 becomes "H". The signal at pin 12 of IC27 becomes "L" and the signal at pin 11 of IC27 becomes "H".
It causes the signal at pin 3 of IC34 becomes "H" from "L". Data fed to pin 2 of IC34 is issued to pin 6 of IC34 while the signal at pin 3 of IC34 rises. Data at pin 2 of IC34 is "L" at that time, and the signal at pin 6 of IC34 becomes "H". Thus, the signal at pin 8 of IC25 becomes "H" to turn on Q27. Thus, $\overline{PSTB}$ causes the printer to start printing data.
Data cannot be received by the printer when the printer is performing a printing operation. In this state, the printer issues BUSY to the controller. BUSY is used to decide whether or not data is to be sent to the printer. BUSY is fed to pin 12 of IC34 through IC25. In this state, $\overline{M1}$ is fed to pin 9 of IC12 (1/4). $\overline{M1}$ informs the controller that operation codes are being fetched by the CPU. The inverted $\overline{M1}$ is fed to pin 11 of IC34. Data appearing at pin 12 of IC34 is issued to pin 9 (Q) of IC34 and then fed to pin 14 of IC55. (BUSY)
$\overline{IORQ}$ is fed to pin 6 of IC52. When the signals at pins 5 and 6 of IC52 become "H", the signal at pin 4 of IC52 becomes "L". $\overline{M1}$ becomes "H" speedily, and thus the signal at pin 4 of IC52 becomes "L" at the end of $\overline{M1}$. It is then fed to pin 2 of IC28.
When both $\overline{IORQ}$ and $\overline{RD}$ are "L", the signal at pin 3 of IC28 is "L". When the signals at pins 2 and 3 of IC28 become "L", the signal at pin 1 of IC28 becomes "H" and then it is fed to pin 1 of IC27.
Pin 13 of IC28 is connected to pin 2 of IC27. Both the input signals at pins 11 and 12 of IC28 are "L" since the I/O port is set in 90H.
Both the signals at pins 1 and 2 of IC27 become "H", the signal at pin 3 of IC27 becomes "L", and the signal at pin 15 of IC55 becomes "L" to send data from pin 14 to pin 13 of IC55. Data is input to microprocessor Z80 so as to check whether or not data is BUSY.



3-7. PROGRAMMABLE PERIPHERAL INTERFACE (PPI) IC16



The diagram above shows the functions of 8255A.
The 8255A is a programmable, general-purpose I/O device designed to construct a 8-bit microcomputer system, and it is characterized by the followings:

(1) An arbitrary function can be selected at the 24 bit I/O terminal by program specification.
(2) Power is supplied from a single 5V power supply.
(3) The direct bit set/reset function is provided.

When $\overline{RD}$ is set active by making it "L" in the read mode or when $\overline{WR}$ is set active by making it "L" in the write mode, data can be transferred between the data bus and each port.

$\overline{CS}$ (CHIP SELECT): By setting $\overline{CS}$ at "L", communication of 8255A with the CPU is permitted. When $\overline{CS}$ set at "H", the data bus has high impedance and control from the CPU is disregarded.

$\overline{WR}$ (WRITE): $\overline{WR}$ is a write enable signal for the 8255A. When $\overline{WR}$ is "L", data or control words can be written into the 8255A.

A_0 and A_1 (PORT ADDRESS): They are used to select and control port A, port B, port C, or the control register when combined with $\overline{RD}$ or $\overline{WR}$. They are also used as low order 2 bits (A_0 and A_1) for the CPU address bus.

RESET: When RESET is "H", data in all registers (including the control register) within the 8255A is cleared.
All the ports are set in the input mode after register contents are cleared.

A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	OPERATION
0	0	0	1	0	PORT A→DATA BUS
0	1	0	1	0	PORT B→DATA BUS
1	0	0	1	0	PORT C→DATA BUS
1	1	0	1	0	NO OPERATION
0	0	0	0	1	DATA BUS→PORT A
0	1	0	0	1	DATA BUS→PORT B
1	0	0	0	1	DATA BUS→PORT C
1	1	0	0	1	DATA BUS→CONTROL REGISTER
×	×	1	×	×	HIGH IMPEDANCE

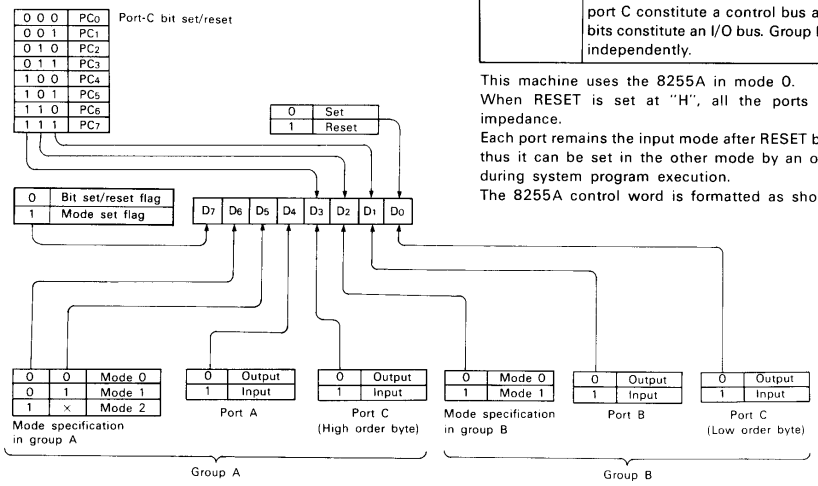
0 ; LOW LEVEL
1 ; HIGH LEVEL
× ; DON'T CASE

A_0, A_1 ; PORT SELECT ADDRESS
$\overline{CS}$; CHIP SELECT
D_0~7 ; DATA BUS
PA_0~7 ; PORT A IN/OUT
PB_0~7 ; PORT B IN/OUT
PC_0~7 ; PORT C IN/OUT
$\overline{RD}$; READ
$\overline{WR}$; WRITE

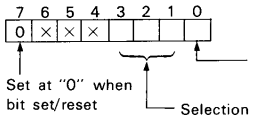
The 8255A provides 3 basic modes one of which can be selected by system software.

(1) Mode 0	Port A	Port B	Port C	
	I/O	I/O	High order byte I/O	Low order byte I/O
(2) Mode 1	Group A		Group B	
	Port A I/O	Port C High order byte I/O (Interrupt control)	Port B I/O	Port C Low order byte I/O (Interrupt control)
(3) Mode 2	Valid only for group A. 8 bits at port A constitute a bidirectional bus. 5 bits in the high order byte at port C constitute a control bus and the remaining bits constitute an I/O bus. Group B can be specified independently.			

This machine uses the 8255A in mode 0.
When RESET is set at "H", all the ports are set at high impedance.
Each port remains the input mode after RESET becomes "L", and thus it can be set in the other mode by an output instruction during system program execution.
The 8255A control word is formatted as shown below.

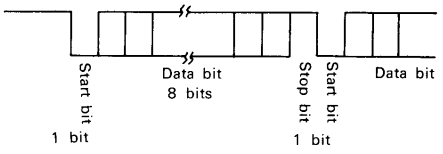


When using C port as an output port, any 1 bit only out of the 8 bits in the C port may be SET (H level)/RESET (L level) with the control word from the CPU.
In this way, the program or data may be SAVEd to the TAPE.



Port C	3	2	1
PC7	1	1	1
PC6	1	1	0
PC5	1	0	1
PC4	1	0	0
PC3	0	1	1
PC2	0	1	0
PC1	0	0	1
PC0	0	0	0

The signal system when recording tape with MSX is performed by FSK modulation and start-stop synchronization (non-synchronization) system. This signal is already generated in the software.
The FSK modulation is a system whereby the frequency of carrier wave may be increased or decreased when the data is either "1" or "0". In the MSX, when the transmitting speed is 1200 buads, it is 1200Hz at "0", and 2400Hz at "1". These are all performed in the software of the MSX. Usually when transmitting or receiving data, it is necessary to set the rules beforehand by the transmitting side and receiving side regarding the data system and the transmission and receiving procedures. The start-stop synchronization system is a system whereby the start bit is firstly placed at the head of the data, and nextly comes the data of the predetermined number of bits and the parity bit, and followed lastly by the stop bit.
In the MSX, a single data is transmitted by 10 bits which are comprised of 1 bit of start bit, 8 bits of data bits and 1 bit of stop bit.
The CPU sends these signals through PPI (IC16).



3-8. PROGRAMMABLE SOUND GENERATOR (PSG) IC48

The IC48 at PSG is possible to make sounds through 3 channels with a single IC, and may also generate noise.
The interior of the PSG is arranged in the manner shown in the diagram on the next page.
Register 0 to 5 determine the frequency of each respective channels and are called channel A, channel B and channel C. As registers 1, 3,and 5 are divided by 4 bits, the values of 0 to 15 are input into these registers. As registers 0, 2, and 4 are divided by 8 bits, the values of 0 to 255 are input into these registers.
Register 6 determines the noise frequency and is divided by 5 bits, the values of 0 to 31 are input into this register.
Register 7 is a switch, and it performs the ON/OFF of the sound of the respective channels or generates noise only.
As this register is negative logic, it becomes activated at "L". When all are turned ON they become 00_H, and when all are turned OFF they become $3F_H$.
Registers 8, 9, and 10 are for use in adjusting the volume of the respective channels, and when bit 4 is "0" volume adjustment in 16 stages may be performed with bits 0 to 3.
When bit 4 is at "1", bits 0 to 3 are ignored and the volume and output systems of the respective channels will vary with the use of an envelope oscillator.
Registers 11 and 12 determine the envelope frequency. Adjustments are performed respectively with 8 bits each.
Register 13 is a place where the system of the envelope waveforms are altered, and as it is comprised of 4 bits the values of 0 to 15 are input.
In order to write in the value to the respective registers or to read out the values of same, they are controlled by signals A_0 and A_1 which are added to pin 29 (BC1) and pin 27 (BDIR).
Register 14 controls I/O port A, and register 15 controls I/O port B.

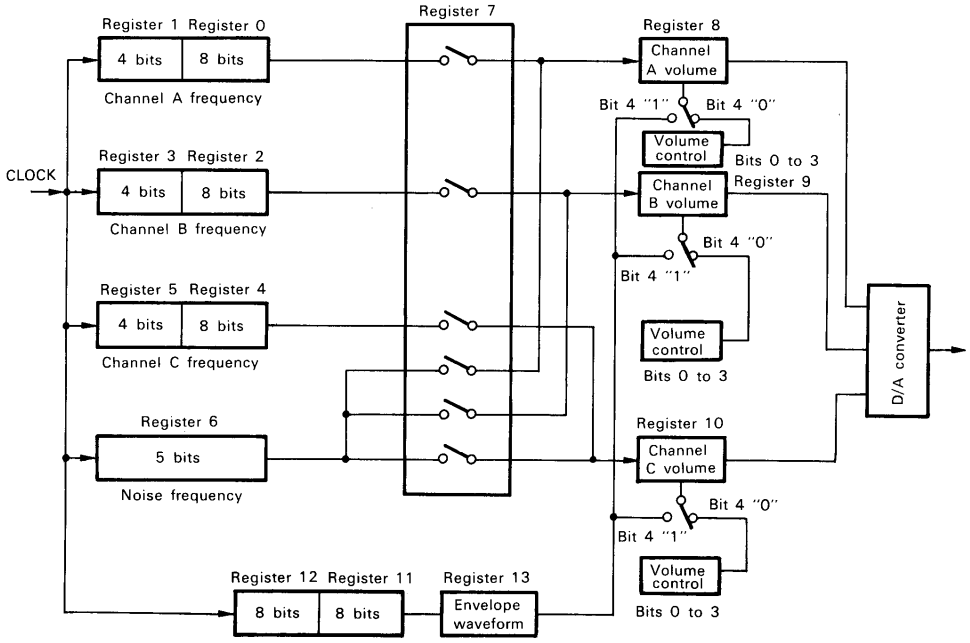
The combinations of A_0 and A_1 are as follows:

A_1	㉗ (BDIR)	㉙ A_0	(BCI)	
0	(1)	0	(1)	Specifies register.
0	(1)	1	(0)	Writes in value to register.
1	(0)	0	(1)	The contents of the register are output to data bus.
1	(0)	1	(0)	Not operated.

The output signals are output to the respective channels from pins 3 , 4 and 38 .
These signals are combined together and amplified with Q26.
The output from the address decoder is connected to pin 4 of IC24, and when PSG is selected it becomes "L". In addition, pin 5 is connected to $\overline{IORQ}$ and when it becomes "L", pin 6 becomes "L".
Therefore, pin 9 of IC52 and pin 11 of IC52 become "L", and operates in the manner stated in the prior clause by A_0 and A_1 of the address bus.

3-8-1. I/O Port of PSG (IC48)

Ther are 2 I/O ports in IC48 and port A is used for input, and port B for output.
These I/O ports may be used as a connector when the joystick is being used.
When the number 7th bit (pin 7) of port B is set at "L", it selects the input from CN8, and when set at "H" it selects the input from CN9.
When the pins 1 of IC62 and IC63 are set at "L", the V0 to Y0 signals appear at the output, and these signals are added to port A of IC48.
When the pins 1 of IC62 and IC63 are set at "H", the V1 to Y1 signals are added to IC48.



3-9. VIDEO DISPLAY PROCESSOR (VDP) IC6

The functions of this IC are as follows:

- Resolution of 256×192 bits
- Uses 4K, 8K, and 16K dynamic RAMs.
- Function of automatic refresh of dynamic video RAM
- Displays 16 colors including black, white and transparent
- Color difference signal output of PAL system
- Occurence of interruption of each frame is possible.
- Automatic processing of superimposition of pictures

This IC controls display screens of the family color television and color monitor television. It outputs all video signals, control signals, synchronizing signals, etc., which are based on the PAL system, and performs read/write to VRAM as also refresh.

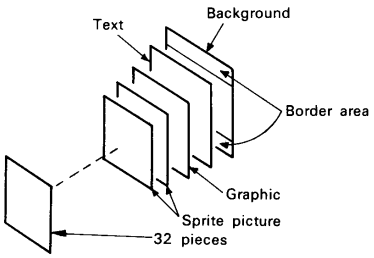
The most distinguished feature of the VDP is the display function of 32 pieces of sprites (graphic pattern of animation pictures). The sprite data registered in the V-RAM are displayed on the sprite surfaces.

These are 8×8 bits or 16×16 bits, and they can be enlarged to twice the sizes of their original sizes.

The color specification (1 color of the 16 colors) of the sprite and the display position are also designated on the VRAM.

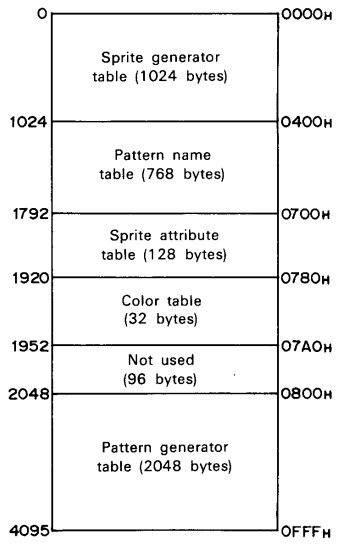
By rewriting this display position coordinates, it can be run at a high speed within the picture.

In accordance with the priority order (#0 is 1st priority) on the surface of the sprite, the low order sprite is erased by the high order sprite, and a 3-dimensional depth effect can be obtained.



3-9-1. VRAM Mapping

The figure below shows an example of the mapping of the VRAM when the sprite and graphic I mode are used. (When used with the MSX, there are some differences according to the types of software used.



① Data area of Graphic I
1) 8×8 bits (8 bytes)
- Maximum 256 kinds
- Maximum 2048 bytes (8 bytes×256)

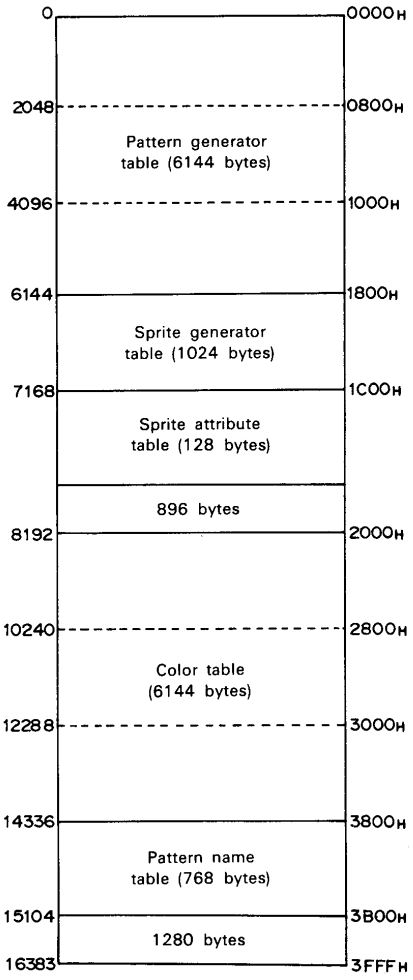
2) Pattern name table
- A table which displays pattern on screen and to store the data which specifies its position.

3) Color table
- A table which stores the color codes of the picture.

② Data area of sprite
1) Sprite attribution table
- Coordinates of sprite
- Selection of display sprite
- Color code specification of sprite

2) Sprite generator table
- Picture data of sprite
- Maximum 256 kinds
- Maximum 2048 bytes (8 bytes×256)

The figure below shows an example of 16K bytes VRAM mapping when graphic II is used. (When used with the MSX, there are some differences according to the types of software used.)



① Data area of Graphic II

1) Pattern generator table
   - 8×8 bits (8 bytes)
   - Maximum 768 (256×3) kinds
   - Maximum 6144 (2048×3) bytes

2) Pattern name table
   - 768 (256×3) bytes

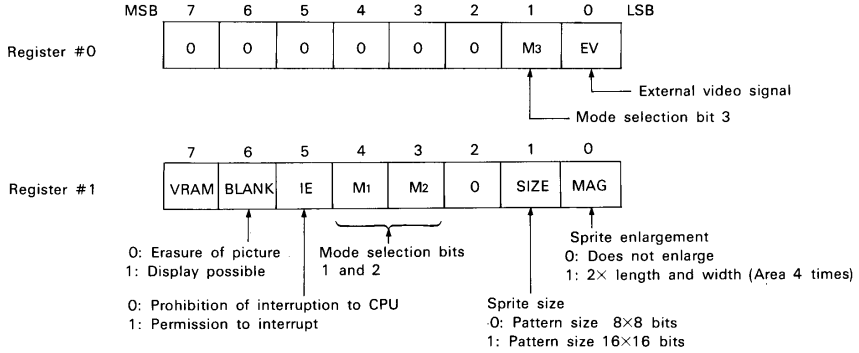
3) Color table
   - Maximum 6144 (2048×3) bytes

3-9-2. VDP Register

In the VDP register, there are a register used exclusively for 8 writing ins and one status register (exclusive to reading out) indicating the state of the VDP.
The picture display is performed by setting data necessary to VDP register, and by writing in picture data to VRAM (dynamic video refresh RAM).

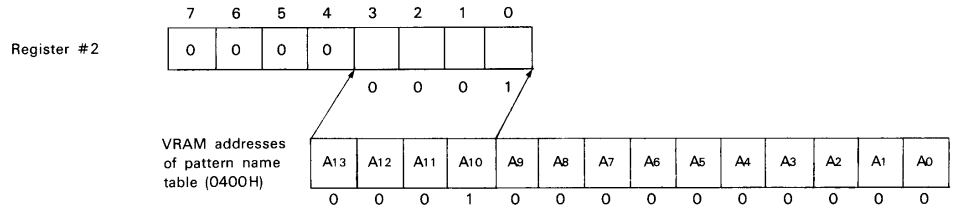
Setting of respective registers:

① **Register #0 and #1**



M1	M2	M3	Display mode
0	0	0	Graphic I
0	0	1	Graphic II
0	1	0	Multi-color
1	0	0	Text

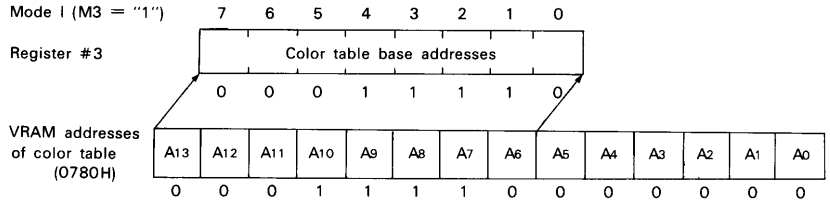
② **Register #2**
Initial setting of pattern name table



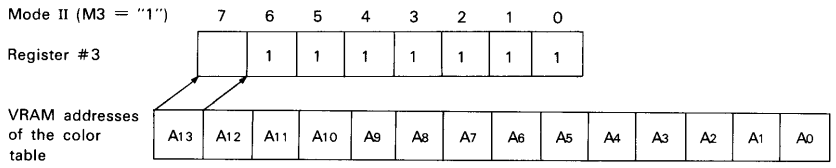
As the VRAM of VDP is up to 16K bytes (3FFH) only and can be shown with 14 bits, the VRAM addresses become as shown in above figure.
Set the upper 4 bits of the VRAM addresses to the lower 4 bits of Register #2. When the pattern name table starts from address>400H $(1024)_{10}$, the content of Register #2 becomes 01.

③ **Register #3**

Initial setting of color table



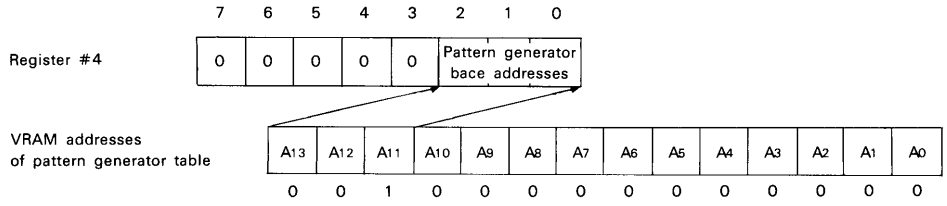
Set upper 8 bits at the head of the addresses of the VRAM color table to Register #3.
When the color table starts from address>780H (1290)10, the value of register #3 becomes 1E.



Set the uppermost bit of the head address of VRAM color table to the uppermost bit of Register #3, and set the rest of the 7 bits all to "1".
When color table is above 2000H, Register #3 becomes FFH.
When it is below 2000H, it becomes 7FH.

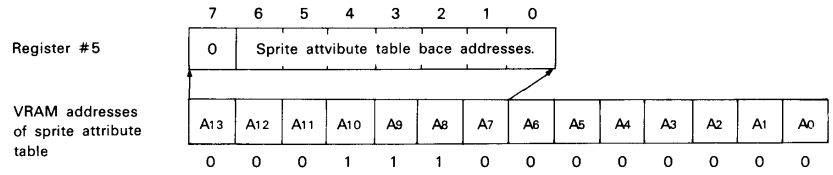
④ **Register #4**

Initial setting of pattern generator table



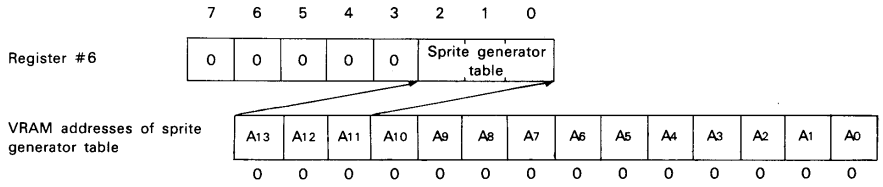
Set upper 3 bits of the head address of VRAM pattern generator table to lower 3 bits of register #4.
When the pattern generator table starts from address>800H (2048)10, the value of register #4 becomes>01.

⑤ **Register #5**
Initial setting of sprite attribution table



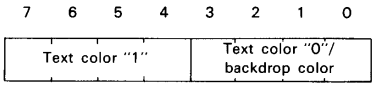
Set upper 7 bits of the head address of VRAM sprite attribution table to lower 7 bits of register #5.
When the sprite attribution table starts from address>700H $(1792)_{10}$, the value of register #5 becomes>0E.

⑥ **Register #6**
Sprite generator table



Set upper 3 bits of the head address of VRAM sprite generator table to lower 3 bits of register #6.
When the sprite generator table starts from address 0, the value of register #6 becomes>00.

⑦ **Register #7**
Setting of text color/backdrop color



Performs the specification of colors when the text mode is selected.
The upper 4 bits specify the color of character data "1", the lower 4 bits specify the color of character data "0" and the color of the backdrop.
When mode other than text mode is specified, the lower 4 bits become backdrop color specification. The VDP color specification is carried out by 16 kinds of codes; namely, from $0 to $F.
The correspondence of the respective codes and colors is as follows:

Code	Color	Code	Color
0	Transparent	8	Medium red
1	Black	9	Light red
2	Medium green	A	Dark yellow
3	Light green	B	Light yellow
4	Dark blue	C	Dark green
5	Light blue	D	Magenta
6	Dark red	E	Gray
7	Sky blue	F	White

3-9-3. VDP Status Register (for reading out only)

7	6	5	4	3	2	1	0
F	5S	C	No. 5 sprite number				

① **Interruption flag (F)**
When IE (No.5 bit) of register #1 is set at "1", the INT output of VDP becomes active ("L") when the scanning of the picture has ended.

② **5S and No.5 sprite number**
When sprites of more than 5 exist in the same horizontal line and the interruption flag (F) is "0", the "5S" bit will be set at "1".
In addition, the number of the No.5the sprite surface will be maintained at lower 5 bits.

③ **Collision flag (C)**
When 1 picture element of more than 2 sprites collide (in accord), it is set at "1".

3-9-4. Reset of VDP Status Register

The status register is reset in the following cases.
1) Input of external reset signal.
2) Reading out of status register
When the flag is once set, it is continuously set unless the reading out of the next status register is performed.

3-9-5. Writing In to the VDP Register

Write in data such as function selection of display mode of the VDP register (for writing in only) and establishment of the respective base addresses.
The transmission of data from the CPU is carried out in the following way.

	Bits 7	6	5	4	3	2	1	0	Control signals $\overline{CSW}$	$\overline{CSR}$	MODE
No.1 byte: Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L	H	H
No.2 byte: Selection of register	1	0	0	0	0	RS_0	RS_1	RS_0	L	H	H

Transmit data with No. 1 byte.
The No.2 byte specifies the register of the receiving end of data at lower 3 bits. The uppermost bit should be "1", and the next 4 bits should be "0".

Control signals
$\overline{CSW}$: When writing in to VDP the 8 bits data (D_0 to D_7) from the CPU, it becomes active ("L").
The data is set to VDP during the rising time of this signal.
$\overline{CSR}$: When it is active ("L"), the VDP outputs the 8 bits (D_0 to D_7) to bus line.
MODE: Set at "L" when transferring data from CPU to VRAM, or when transferring data from VRAM to CPU. In cases other than above, set at "H".

3-9-6. Writing In to VRAM

The CPU transfers data to VRAM after going through VDP, with the 14 bit automatic increment address register stored within the VDP.
It is necessary to use 2 bytes in setting up this address register. Figure below shows how to set up this address register and perform data transfer.

		Control signal $\overline{CSW}$	$\overline{CSR}$	MODE
No.1 byte: Address set up	A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	L	H	H
No.2 byte: Address set up	0 1 A_{13} A_{12} A_{11} A_{10} A_9 A_8	L	H	H
No.3 byte: Data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	L	H	L

Set up the lower 8 bits of VRAM address with No.1 byte.
Set up upper 6 bits with No.2 bytes.
At this time, the upper 2 bits are (01). Transmit data with No.3 byte.
Once the address register is set up, it is automatically incremented every time the next No.3 byte transfers data.
The MODE signal is set at "H" when transferring address, and at "L" when transferring data.

3-9-7. Reading Out of Status Register

The CPU performs the reading out with 1 byte the contents of the status register. The respective control signals at this time are as follows:

	Bits 7	6	5	4	3	2	1	0	Control signals $\overline{CSW}$	$\overline{CSR}$	MODE
Status register data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	H	L	H

3-9-8. Reading Out from the VRAM

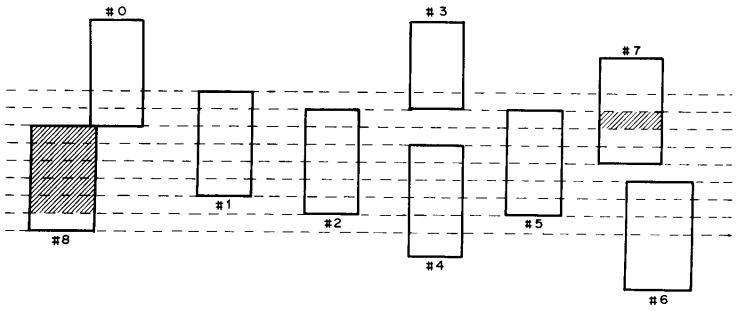
The CPU reads out the data from VRAM after going through VDP. Addresses are automatically incremented.

		Control signals $\overline{CSW}$	$\overline{CSR}$	MODE
No.1 byte: Address set up	A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	L	H	H
No.2 byte: Address set up	0 0 A_{13} A_{12} A_{11} A_{10} A_9 A_8	L	H	H
No.3 byte: Data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	H	L	L

This device employs the I/O ports 98H to 99H for VDP use.
The control signals $\overline{CSW}$ and $\overline{CSR}$ of IC6 (VDP) become active when $\overline{IORQ}$ and $\overline{RD}$ or $\overline{WR}$ become "L" when the address bus signal is 98H or 99H.
When $\overline{IORQ}$ and $\overline{RD}$ are "L", $\overline{CSR}$ becomes active.
When $\overline{IORQ}$ and $\overline{WR}$ are "L", $\overline{CSW}$ becomes active.
When the address bus signal is 98H, it is accessed to VRAM.
When the address bus signal is 99H, it is accessed to VDP register.

3-9-9. Display Limitation of Sprite

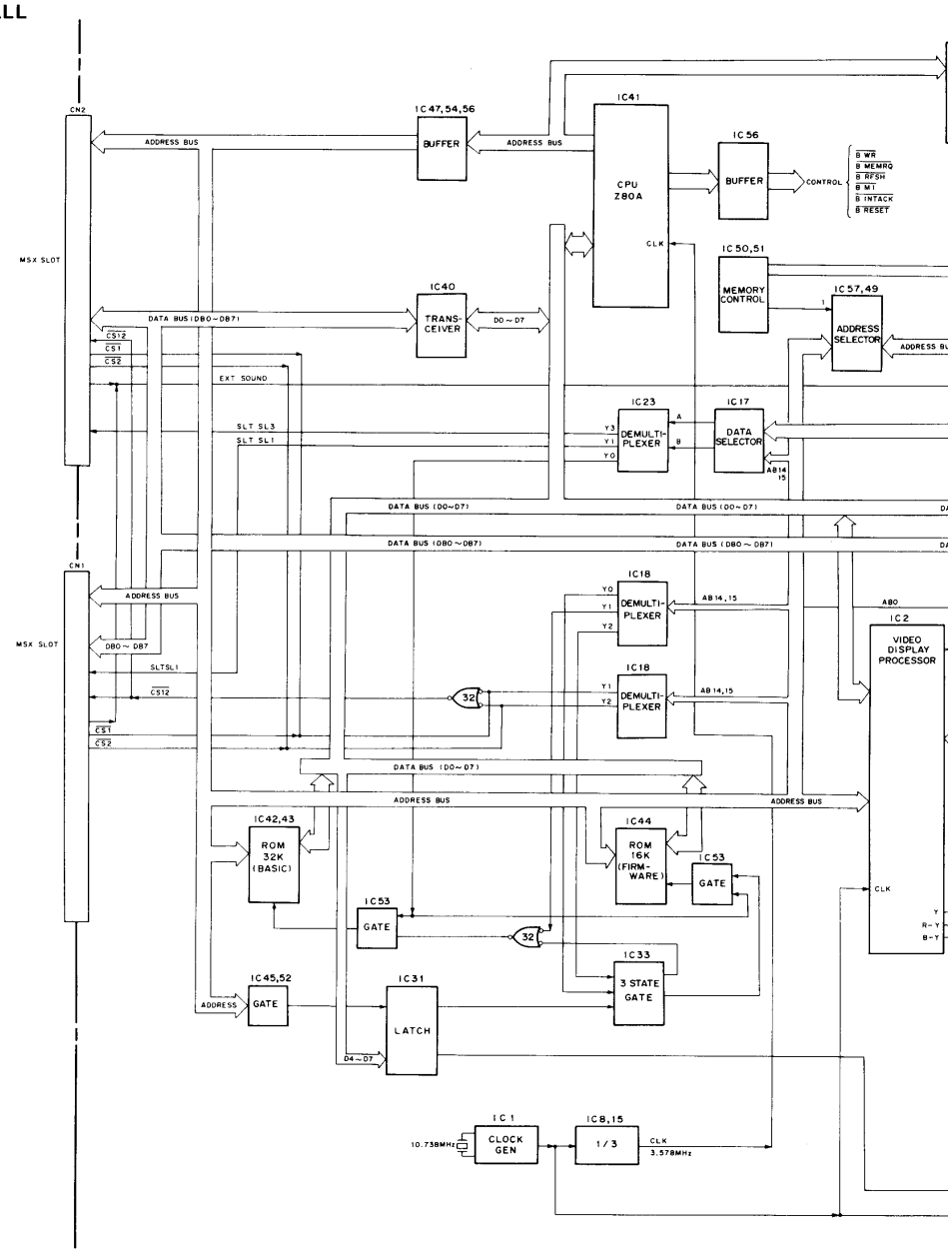
The hatched portion becomes transparent and the background pattern is displayed.

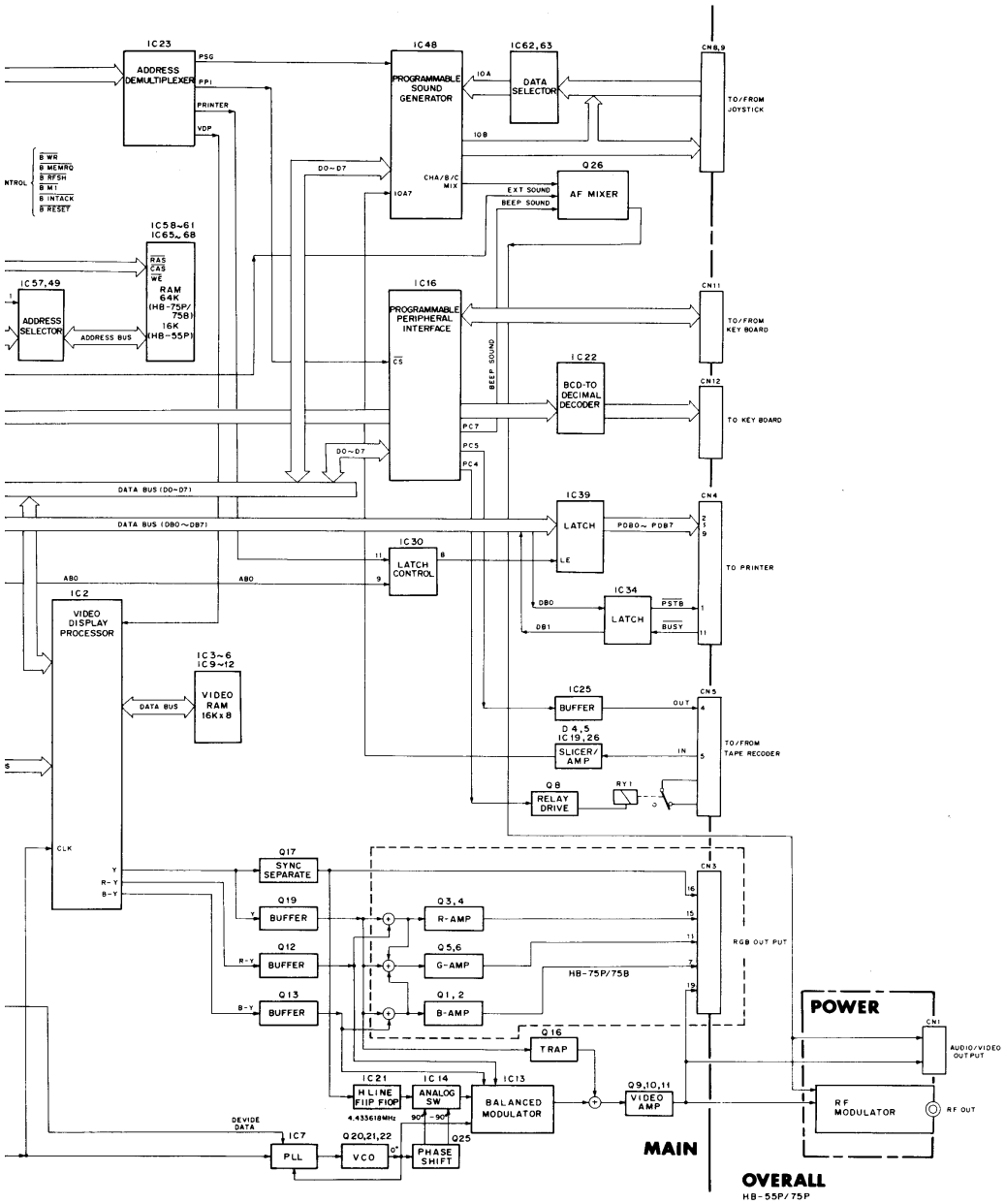


① The sprites up to 4 can take place on a same horizontal line.
② When the sprites of more than 5 take place on the same horizontal line, 4 sprites that have high priority (in the order of #0, #1 . . . . . #32) are displayed and the sprite from 5 and above are not displayed.
③ The state of the sprites can be ascertained by referring to the status register.

CHAPTER 4
BLOCK DIAGRAM

OVERALL

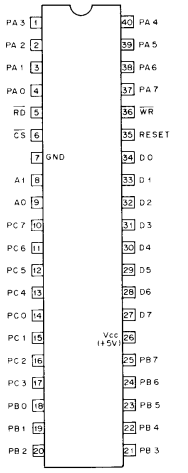



IC23
ADDRESS DEMULTIPLEXER
PSG
PPI
PRINTER
VDP
IC48
PROGRAMMABLE SOUND GENERATOR
IOA
IOB
IOA7
CHA/B/C MIX
IC62,63
DATA SELECTOR
CN8,9
TO/FROM JOYSTICK
Q26
AF MIXER
EXT SOUND
BEEP SOUND
D0~D7
IC58~61
IC65~68
RAM 64K (HB-75P/75B) 16K (HB-55P)
IC57,49
ADDRESS SELECTOR
ADDRESS BUS
IC16
PROGRAMMABLE PERIPHERAL INTERFACE
CS
BEEP SOUND
PC7
PC5
PC4
CN11
TO/FROM KEY BOARD
IC22
BCD-TO DECIMAL DECODER
CN12
TO KEY BOARD
DATA BUS (D0~D7)
DATA BUS (DB0~DB7)
IC39
LATCH
LE
PDB0~ PDB7
CN4
TO PRINTER
IC30
LATCH CONTROL
A8
IC34
LATCH
DB0
DB1
PSTB
BUSY
IC2
VIDEO DISPLAY PROCESSOR
IC3~6
IC9~12
VIDEO RAM 16K x 8
DATA BUS
IC25
BUFFER
OUT
CN5
TO/FROM TAPE RECODER
D4,5
IC19,26
SLICER/ AMP
IN
Q8
RELAY DRIVE
RY1
CLK
Y
R-Y
B-Y
Q17
SYNC SEPARATE
Q19
BUFFER
Q12
BUFFER
Q13
BUFFER
Q3,4
R-AMP
Q5,6
G-AMP
Q1,2
B-AMP
HB-75P/75B
CN3
RGB OUT PUT
POWER
CN1
AUDIO/VIDEO OUT PUT
RF MODULATOR
RF OUT
Q16
TRAP
IC21
H LINE FIIP FIOP
4.433618MHz
IC14
ANALOG SW
90°-90°
IC13
BALANCED MODULATOR
Q9,10,11
VIDEO AMP
DEVIDE DATA
IC7
PLL
Q20,21,22
VCO
Q25
PHASE SHIFT
MAIN
OVERALL
HB-55P/75P
HB-75B

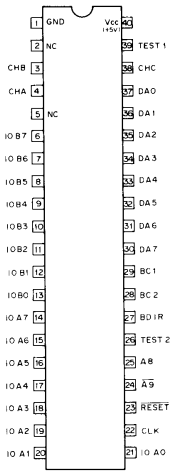
CHAPTER 5
SCHEMATIC DIAGRAM AND PRINTED CIRCUIT BOARD

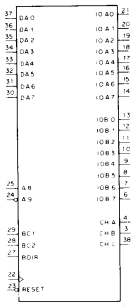
SEMICONDUCTOR PIN ASSIGNMENTS

μPD8255AC-5 (NEC)
PROGRAMMABLE PERIPHERAL INTERFACE
— TOP VIEW —

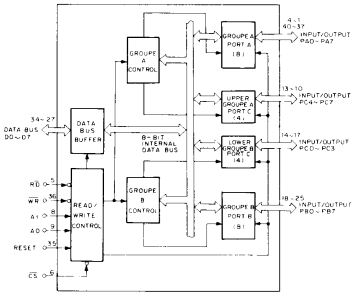


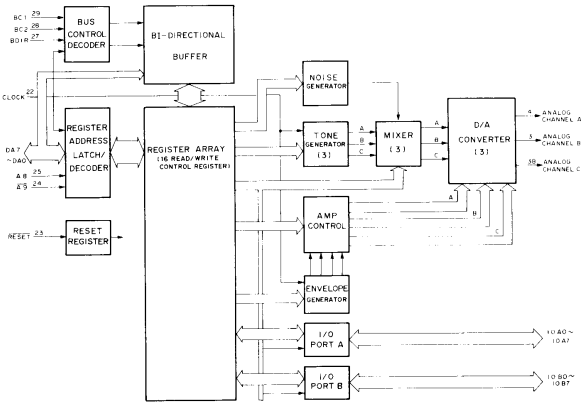
AY-3-8910 (GENERAL INSTRUMENT)
YM-2149 (YAMAHA)
PROGRAMMABLE SOUND GENERATOR
— TOP VIEW —





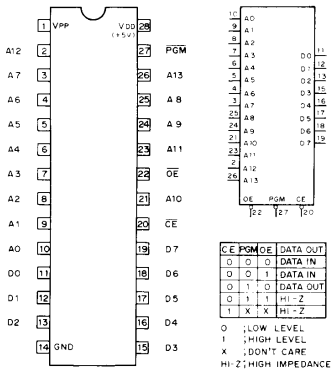
BC1, 2; BUS CONTROL 1, 2
BDIR; BUS DIRECTION
CHA~CHC; ANALOG CHANNEL
CLK; CLOCK
DA0~DA7; DATA ADDRESS
IOA0~IOA7; INPUT/OUTPUT A
IOB0~IOB7; INPUT/OUTPUT B
RESET; RESET





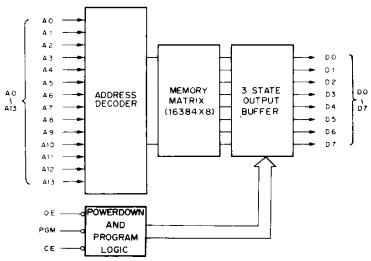
HN4827128G-25 (HITACHI) (ACCESS TIME = 250nS)
HN4827128G-30 (HITACHI) (ACCESS TIME = 300nS)

N-MOS ERASABLE AND PROGRAMMABLE ROM 128K-BIT (16384x8)
— TOP VIEW —



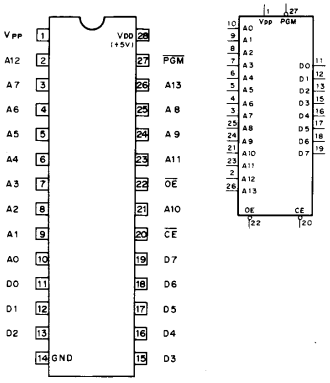
CE	PGM	OE	DATA OUT
0	0	0	DATA IN
0	0	1	DATA IN
0	1	0	DATA OUT
0	1	1	HI-Z
1	X	X	HI-Z

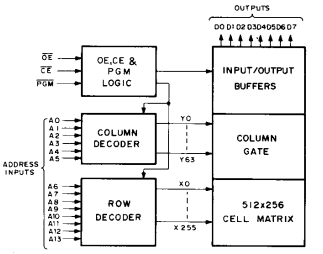
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE



A0-13 ; ADDRESS INPUT
CE ; CHIP ENABLE
D0-7 ; DATA
OE ; OUTPUT ENABLE
PGM ; PROGRAM

MBM27128 (FUJITSU)
N-MOS UV EPROM 128K-BIT (16384x8)
— TOP VIEW —

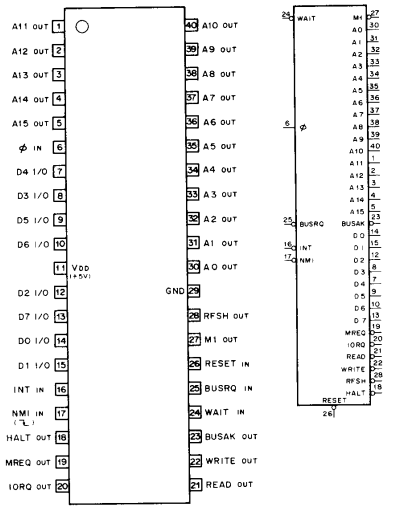


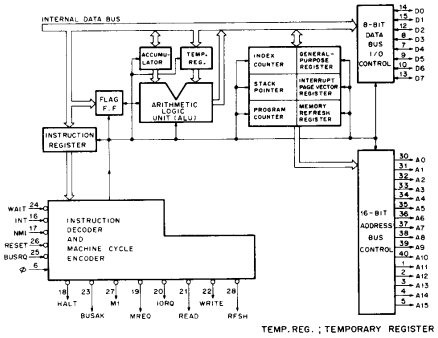


TERMINAL MODE	CE	OE	PGM	VPP	Vcc	OUTPUTS
READ	0	0	1	+5V	+5V	DATA OUT
STAND-BY	1	X	X	+5V	+5V	HIGH IMPEDANCE
PROGRAMMING	0	1	0	+21V	+21V	DATA IN
PROGRAM VERIFY	0	0	1	+21V	+5V	DATA OUT
PROGRAM INHIBIT	1	X	X	+21V	+5V	HIGH IMPEDANCE
HIGH SPEED PROGRAMMING	0	1	0	+21V	+6V	DATA IN

1 ; TTL LEVEL HIGH VOLTAGE IN
0 ; TTL LEVEL LOW VOLTAGE IN
X ; DON'T CARE (1 OR 0)

LH0080A (SHARP)
uPD780C-1 (NEC)
N-MOS 8-BIT MICROPROCESSOR
— TOP VIEW —

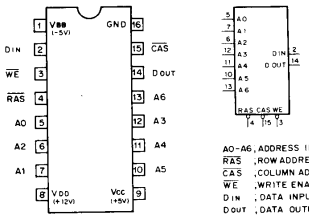




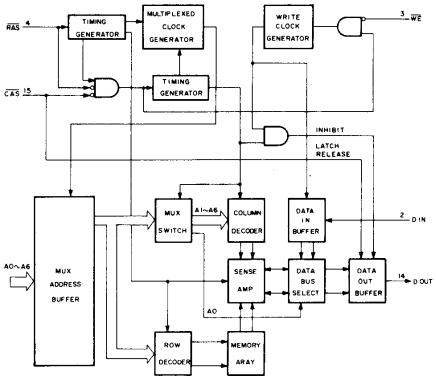
TEMP. REG. ; TEMPORARY REGISTER

φ ; CLOCK
A0-A15 ; 3-STATE ADDRESS OUTPUT
BUSAK ; BUS ACKNOWLEDGE
BUSRQ ; BUS REQUEST
D0-D7 ; 3-STATE DATA INPUT/OUTPUT
HALT ; HALT STATE
INT ; INTERRUPT REQUEST
IORQ ; 3-STATE I/O REQUEST
M1 ; MACHINE CYCLE 1
MREQ ; 3-STATE MEMORY REQUEST
NMI ; NON-MASKABLE INTERRUPT (DOWN EDGE TRIGGER)
READ ; 3-STATE MEMORY READ
RFSH ; REFRESH
WRITE ; 3-STATE MEMORY WRITE

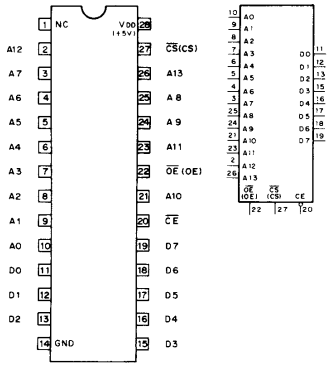
MCM4116BP20 (MOTOROLA) (ACCESS TIME = 200 nS)
uPD416C-2 (NEC) (ACCESS TIME = 200 nS)
N-MOS 16384-WORD BY 1-BIT DYNAMIC RAM
— TOP VIEW —



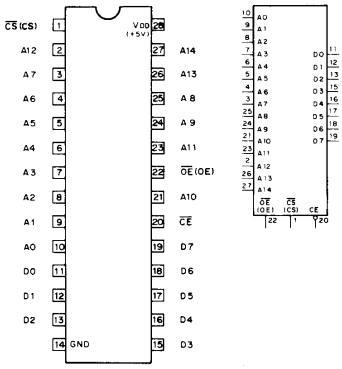
A0-A6, ADDRESS INPUT
RAS ,ROW ADDRESS STROBE INPUT
CAS ,COLUMN ADDRESS STROBE INPUT
WE ,WRITE ENABLE
DIN , DATA INPUT
DOUT , DATA OUTPUT

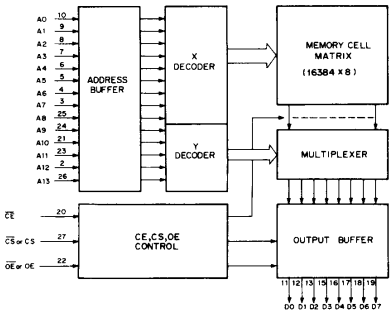


MSM38128ARS (OKI)
N-MOS MASK PROGRAMMABLE ROM 128K-BIT (16384x8)
— TOP VIEW —

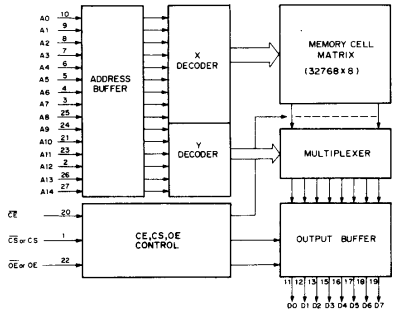


MSM38256RS (OKI)
N-MOS MASK PROGRAMMABLE ROM 256K-BIT (32768x8)
— TOP VIEW —



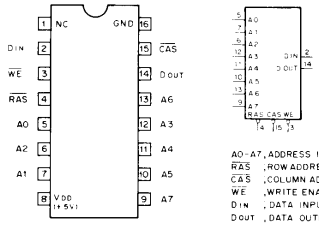


A0 ~ A12 ; ADDRESS INPUT
CE ; CHIP ENABLE
CS ; CHIP SELECT
D0 ~ D7 ; DATA
OE ; OUTPUT ENABLE

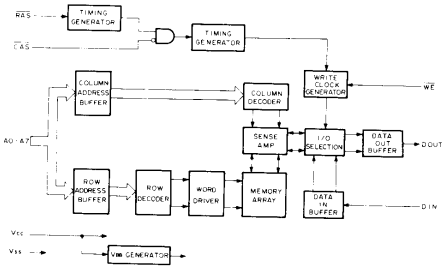


A0 ~ A14 ; ADDRESS INPUT
CE ; CHIP ENABLE
CS ; CHIP SELECT
D0 ~ D7 ; DATA
OE ; OUTPUT ENABLE

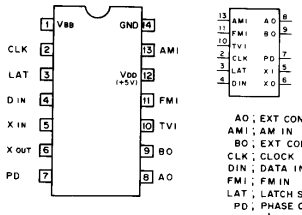
HM4864P-2 (HITACHI) (ACCESS TIME = 150 nS)
HM4864P-3 (HITACHI) (ACCESS TIME = 200 nS)
MSM3764-15RS (OKI) (ACCESS TIME = 150 nS)
MSM3764-20RS (OKI) (ACCESS TIME = 200 nS)
N-MOS 65,536-WORD BY 1-BIT DYNAMIC RAM
— TOP VIEW —



AO-A7, ADDRESS INPUT
$\overline{RAS}$; ROW ADDRESS STROBE INPUT
$\overline{CAS}$; COLUMN ADDRESS STROBE INPUT
$\overline{WE}$; WRITE ENABLE
DIN ; DATA INPUT
DOUT ; DATA OUTPUT

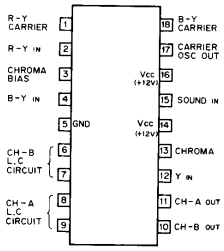


CX7925A (SONY) (MAX 300MHz)
CX7925A-1 (SONY) (MAX 350MHz)
N MOS PLL
— TOP VIEW —

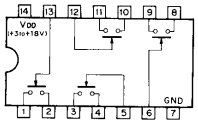


AO ; EXT CONTROL
AMI ; AM IN
BO ; EXT CONTROL
CLK ; CLOCK
DIN ; DATA INPUT
FMI ; FM IN
LAT ; LATCH SIGNAL INPUT
PD ; PHASE COMPARATOR OUT
XI,XO ; X'TAL INPUT

LM1889N (NSC)
TV VIDEO MODULATOR
— TOP VIEW —

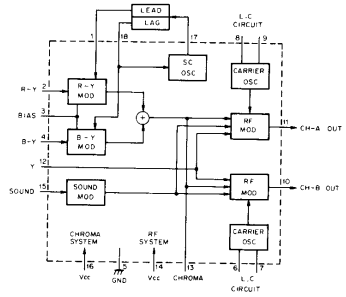


HD14066BP (HITACHI)
uPD4066BC (NEC)
C-MOS BILATERAL SWITCH
— TOP VIEW —

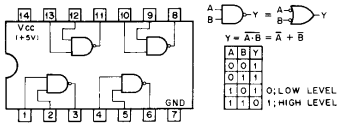


CONT IN	SW
0	OFF
1	ON

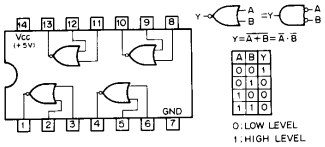
0 ; LOW LEVEL
1 ; HIGH LEVEL



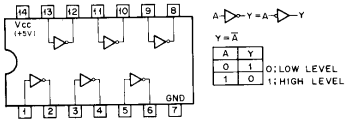
MB74LS00 (FUJITSU)
SN74LS00N (TI)
TTL 2-INPUT POSITIVE-NAND GATE
— TOP VIEW —



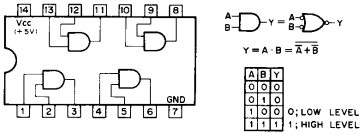
MB74LS02 (FUJITSU)
SN74LS02N (TI)
TTL 2-INPUT POSITIVE-NOR GATE
— TOP VIEW —



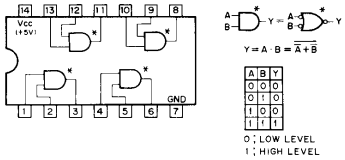
MB74LS04 (FUJITSU)
SN74LS04N (TI)
TTL INVERTER
— TOP VIEW —



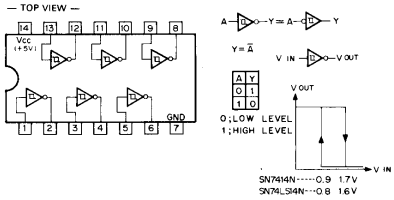
MB74LS08 (FUJITSU)
SN74LS08N (TI)
TTL 2-INPUT POSITIVE-AND GATE
— TOP VIEW —



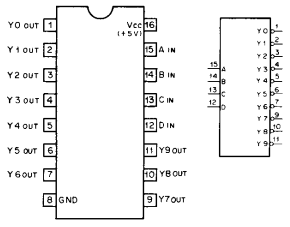
MB74LS09 (FUJITSU)
SN74LS09N (TI)
TTL 2-INPUT POSITIVE-AND GATE WITH OPEN-COLLECTOR
— TOP VIEW —



MB74LS14 (FUJITSU)
SN74LS14N (TI)
TTL SCHMITT TRIGGER INVERTER
— TOP VIEW —



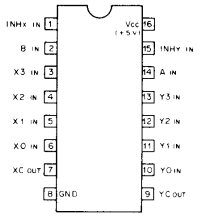
MB74LS145 (FUJITSU)
SN74LS145N (TI)
TTL BCD-TO-DECIMAL DECODER/DRIVER
— TOP VIEW —

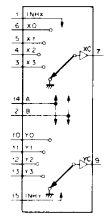


STATE	INPUTS				OUTPUTS								
	D	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	1	1
2	0	0	1	0	1	1	0	1	1	1	1	1	1	1
3	0	0	1	1	1	1	1	0	1	1	1	1	1	1
4	0	1	0	0	1	1	1	1	0	1	1	1	1	1
5	0	1	0	1	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	1	1	1	1	1	0	1	1	1
7	0	1	1	1	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	1	1	1	1	1	1	1	0
INVALID	1	0	1	0	1	1	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	1	1	1	1	1	1	1	1
	1	1	0	0	1	1	1	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	1	1	1	1	1	1
	1	1	1	0	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0 ; LOW LEVEL
1 ; HIGH LEVEL

MB74LS153 (FUJITSU)
SN74LS153N (TI)
TTL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER
— TOP VIEW —

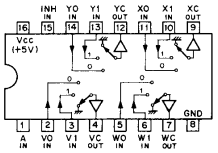


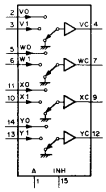


CONTROL IN			ON CHANNEL
INH	B	A	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	GND

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

HD74LS157P (HITACHI)
MB74LS157 (FUJITSU)
SN74LS157N (TI)
TTL 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER
— TOP VIEW —

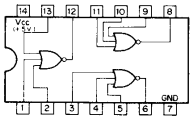


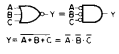


CONT. IN		ON CHANNEL
INH	A	
0	0	0
0	1	1
1	X	GND

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

MB74LS27 (FUJITSU)
SN74LS27N (TI)
TTL 3-INPUT POSITIVE-NOR GATE
— TOP VIEW —

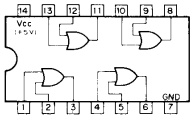


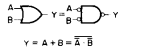


A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL

MB74LS32 (FUJITSU)
SN74LS32N (TI)
TTL 2-INPUT POSITIVE-OR GATE
— TOP VIEW —

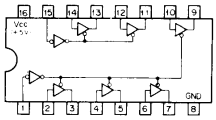




A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

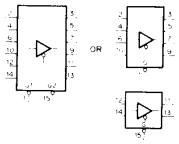
0 ; LOW LEVEL
1 ; HIGH LEVEL

MB74LS367A (FUJITSU)
SN74LS367AN (TI)
TTL BUS DRIVER WITH 3-STATE OUTPUTS
— TOP VIEW —

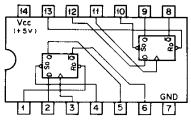


G	A	Y
0	0	0
0	1	1
1	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE



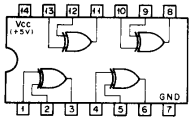
HD74LS74AP (HITACHI)
MB74LS74A (FUJITSU)
SN74LS74AN (TI)
TTL D-TYPE FLIP FLOP WITH DIRECT SET/RESET
— TOP VIEW —



INPUTS				OUTPUTS	
$\overline{S_D}$	$\overline{R_D}$	CK	D	Q_{n+1}	$\overline{Q_{n+1}}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_n	$\overline{Q_n}$

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
1* ; NONSTABLE

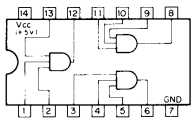
HD74LS86P (HITACHI)
MB74LS86 (FUJITSU)
SN74LS86N (TI)
TTL EXCLUSIVE OR GATE
— TOP VIEW —

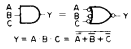


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL

MB74LS11 (FUJITSU)
SN74LS11N (TI)
TTL 3-INPUT POSITIVE-AND GATE
— TOP VIEW —

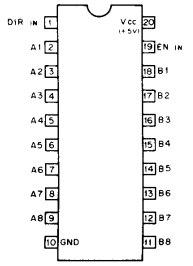




A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

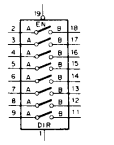
0 ; LOW LEVEL
1 ; HIGH LEVEL

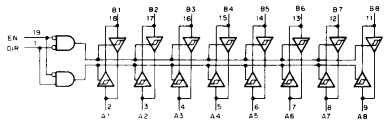
SN74LS245N (TI)
TTL BILATERAL SCHMITT TRIGGER BUS TRANSCEIVERS WITH 3-STATE OUTPUT
— TOP VIEW —



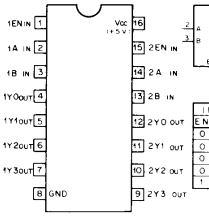
EN	DIR	OPERATION
0	0	B to A
0	1	A to B
1	X	HI-Z

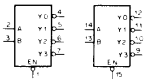
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z, HIGH IMPEDANCE





MB74LS139 (FUJITSU)
SN74LS139N (TI)
TTL 2-TO-4-LINE DECODER/DEMULTIPLEXER
— TOP VIEW —

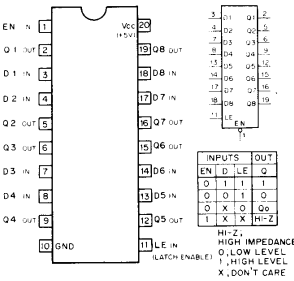




INPUTS			OUTPUTS		
EN	B	A	Y3	Y2	Y1	Y0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

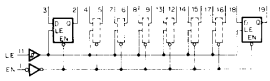
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

HD74LS373P (HITACHI)
MB74LS373 (FUJITSU)
SN74LS373N (TI)
TTL 3-STATE OUTPUTS OCTAL LATCHES
— TOP VIEW —

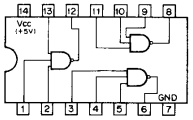


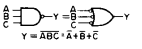
INPUTS			OUT
EN	D	LE	Q
0	1	1	1
0	0	1	0
0	X	0	Q0
1	X	X	HI-Z

HI-Z, HIGH IMPEDANCE
0, LOW LEVEL
1, HIGH LEVEL
X, DON'T CARE



MB74LS10 (FUJITSU)
SN74LS10N (TI)
TTL 3-INPUT POSITIVE NAND GATE
— TOP VIEW —

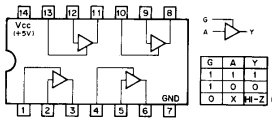




A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL

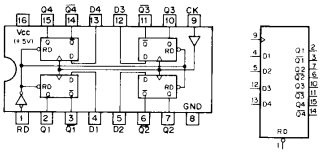
MB74LS126A (FUJITSU)
SN74LS126AN (TI)
TTL BUS BUFFER GATE WITH 3-STATE OUTPUT
— TOP VIEW —



G	A	Y
1	1	1
1	0	0
0	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

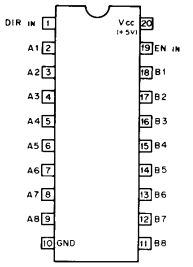
MB74LS175 (FUJITSU)
SN74LS175N (TI)
TTL D-TYPE FLIP-FLOP WITH CLEAR
— TOP VIEW —



RD	CK	D	Q	Q̄
0	X	X	0	1
1	↑	1	1	0
1	↑	0	0	1
1	0	X	Q_0	$\bar{Q}_0$

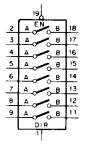
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

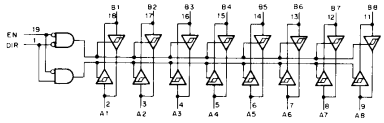
HD74LS645P (HITACHI)
SN74LS645N (TI)
TTL BILATERAL SCHMITT TRIGGER BUS TRANSCEIVERS WITH 3-STATE OUTPUT
— TOP VIEW —



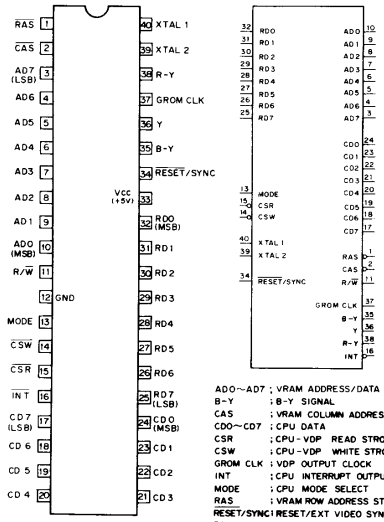
EN	DIR	OPERATION
0	0	B to A
0	1	A to B
1	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

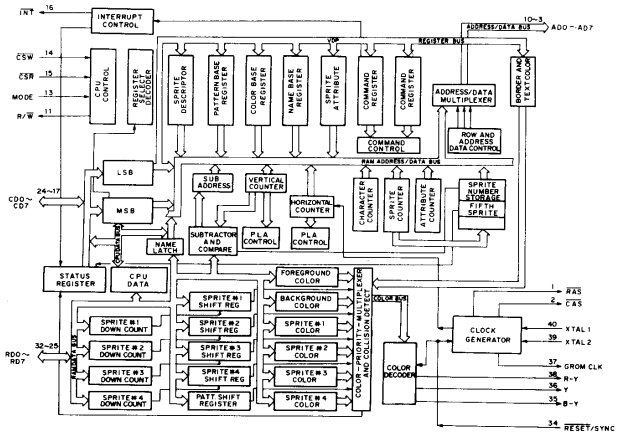




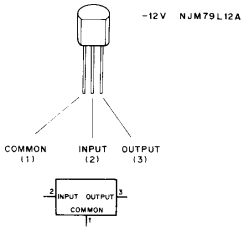
TMS9929ANL (TI) (PAL COLOR-DIFFERENCE SIGNAL)
N-MOS VIDEO DISPLAY PROCESSOR
— TOP VIEW —



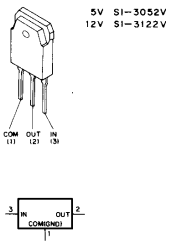
AD0~AD7 ; VRAM ADDRESS/DATA
B-Y ; B-Y SIGNAL
CAS ; VRAM COLUMN ADDRESS STROBE
CD0~CD7 ; CPU DATA
CSR ; CPU-VDP READ STROBE
CSW ; CPU-VDP WHITE STROBE
GROM CLK ; VDP OUTPUT CLOCK
INT ; CPU INTERRUPT OUTPUT
MODE ; CPU MODE SELECT
RAS ; VRAM ROW ADDRESS STROBE
RESET/SYNC ; RESET/EXT VIDEO SYNC
RD0~RD7 ; VRAM READ DATA
R/W ; VRAM READ/WRITE
R-Y ; R-Y SIGNAL
XTAL1,2 ; CRYSTAL INPUT
Y ; Y SIGNAL



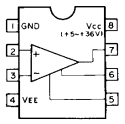
NJM79L ? ?A (JRC)
NEGATIVE VOLTAGE REGULATOR (40mA)
— FRONT VIEW —



SI-3052V (SANKEN)
SI-3122V (SANKEN)
POSITIVE VOLTAGE REGULATOR (2A)

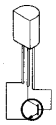


μPC311C (NEC)
VOLTAGE COMPARATOR
— TOP VIEW —

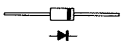


Tr, Di

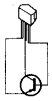
2SA1027R



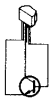
2SC2001



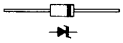
10E-2
1N4148H
1S1555
1S2076
1S2473
1SS119
1SS133
1SS148
1SS202
US1035



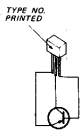
2SA1048
2SA1115



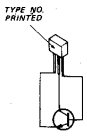
2SC2458
2SC2603
2SD1012



RD ? ?EL



2SA1175



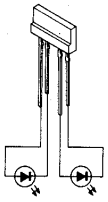
2SC2785
2SD1020

KV1320

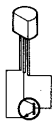
2SA733

2SK30A

RB402



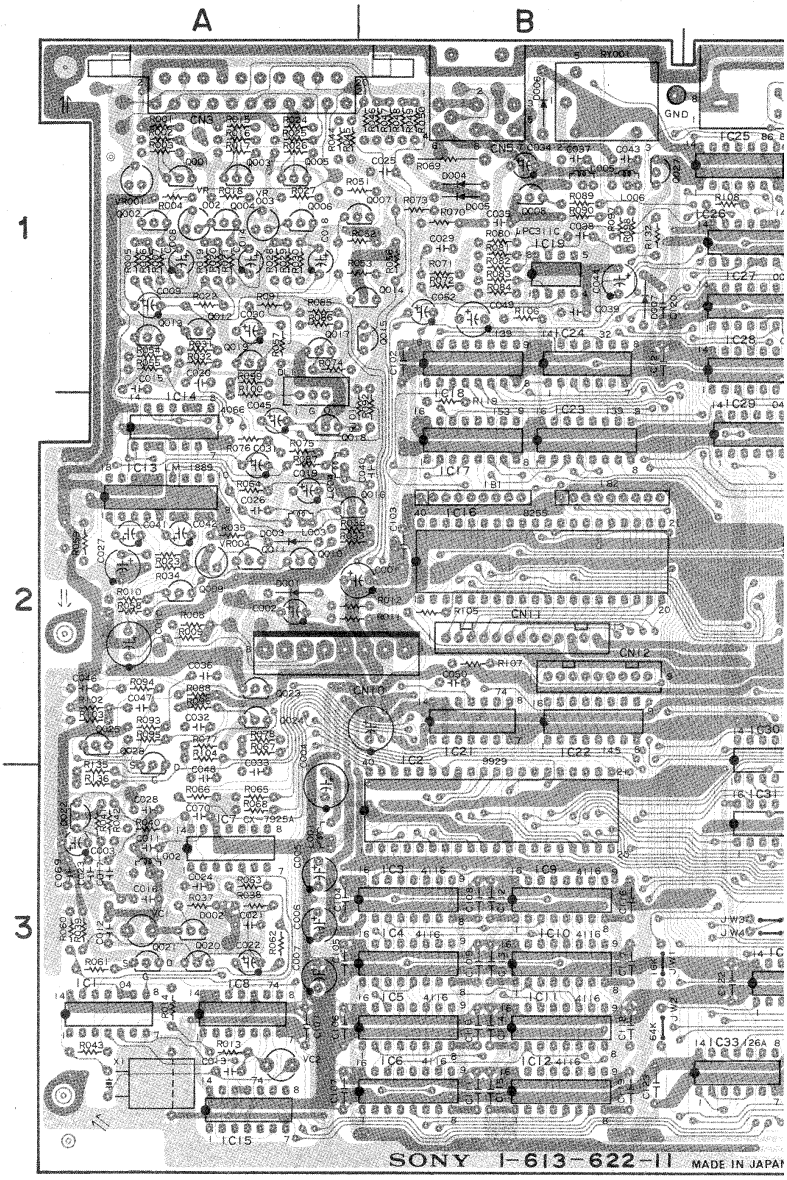
SLP-171D; RED



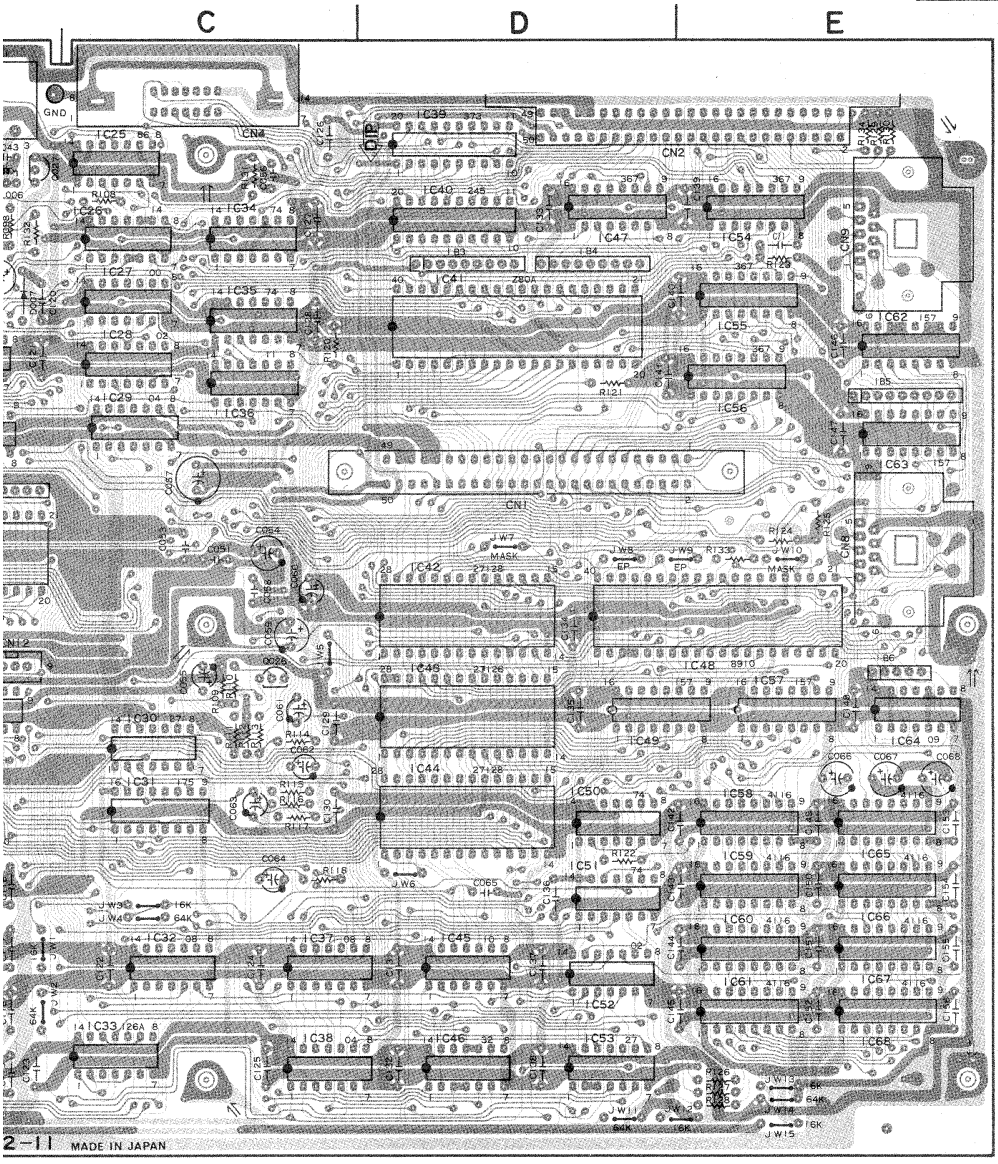
2SC1364
2SC2120
2SC641K
2SC945

MAIN

MAIN BOARD



Note: The blue pattern on board layout is COMPONENT SIDE.
The gray pattern on board layout is SOLDERING SIDE.



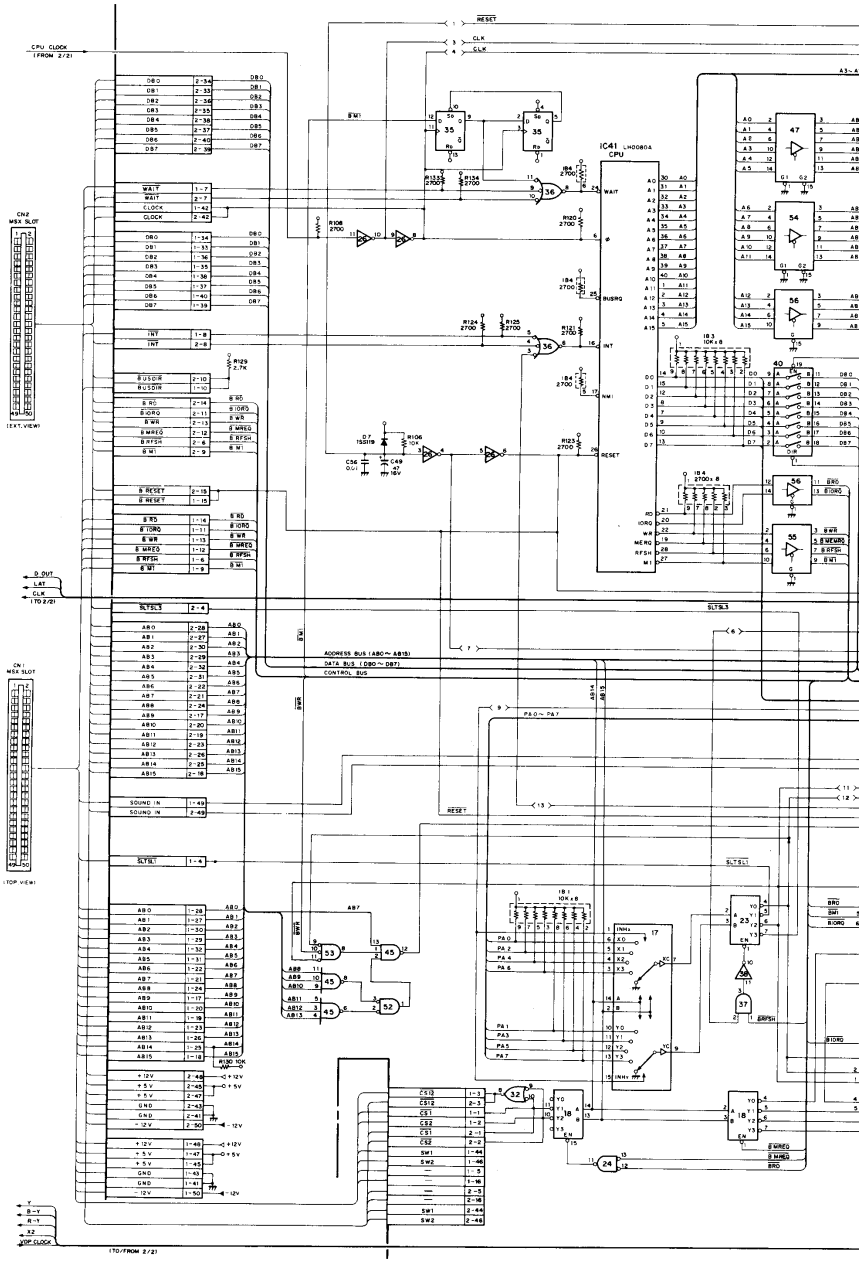
MAIN BOARD – COMPONENT SIDE –

1-613-622-11
HB-55P/75P(AE)
HB-75B(UK)

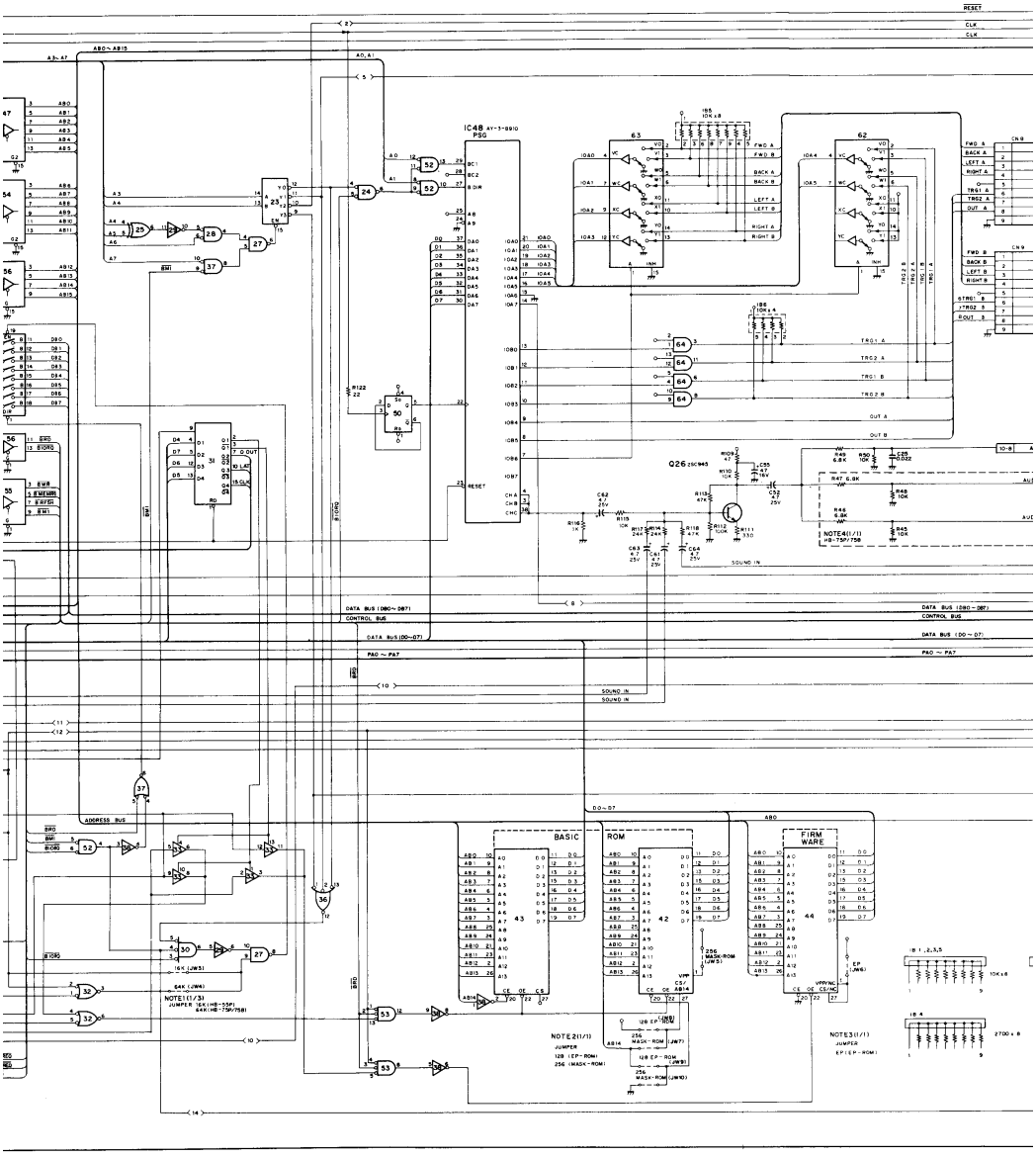
MAIN

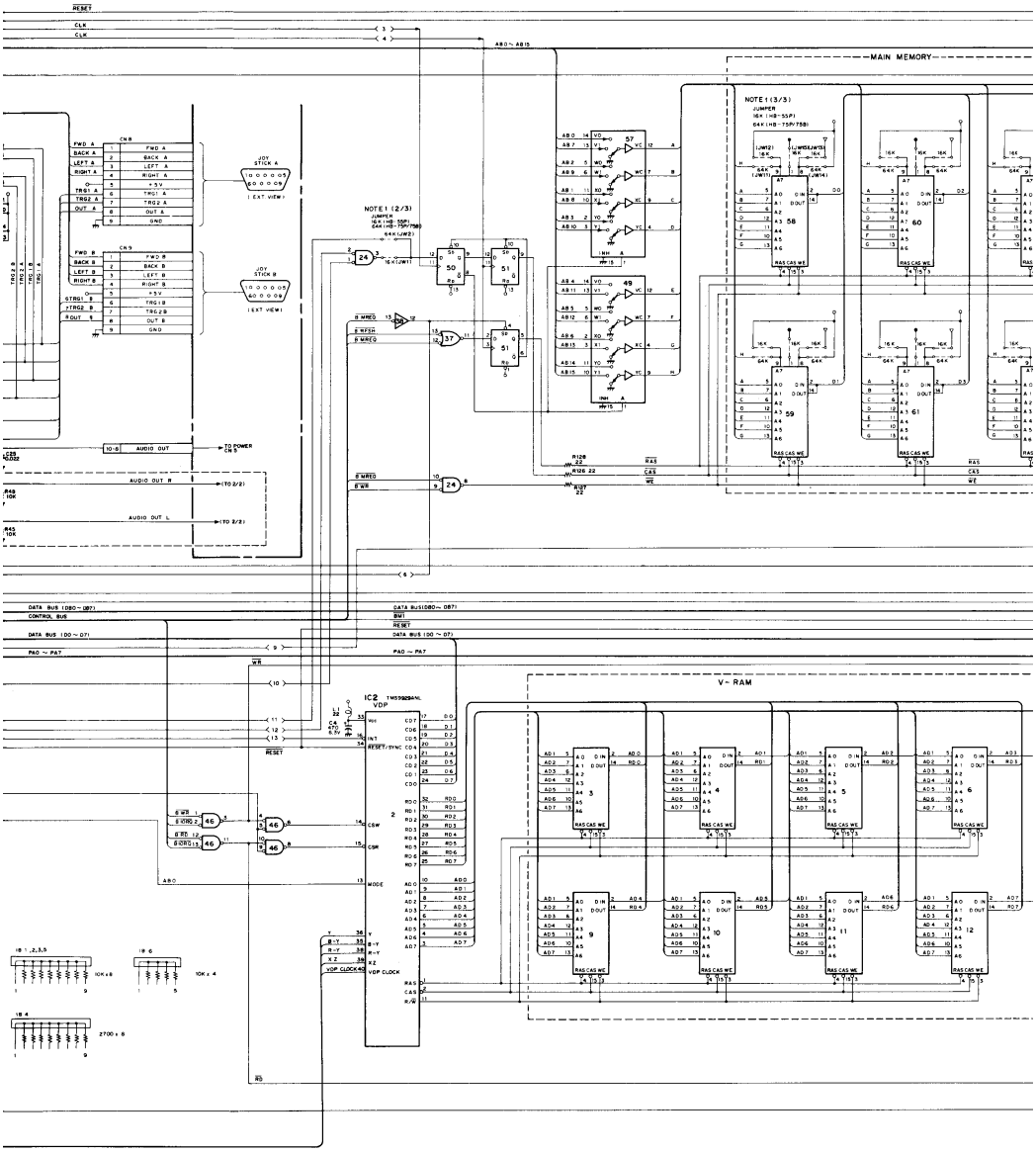
C001	B - 2	C066	E - 3	CN1	D - 2	IC31	C - 3	Q001	A - 1	R036	A - 2	R100	A - 1		
C002	A - 2	C067	E - 3	CN2	E - 1	IC32	C - 3	Q002	A - 1	R037	A - 3	R101	A - 2		
C003	A - 3	C068	E - 3	CN3	A - 1	IC33	C - 3	Q003	A - 1	R038	A - 3	R102	A - 2		
C004	A - 3	C069	A - 3	CN4	C - 1	IC34	C - 1	Q004	A - 1	R039	A - 3	R103	A - 2		
C005	A - 3	C070	A - 3	CN5	B - 1	IC35	C - 1	Q005	A - 1	R040	A - 3	R104	A - 2		
C006	A - 3	C071	E - 1	CN8	E - 2	IC36	C - 1	Q006	A - 1	R041	A - 3	R105	B - 2		
C007	A - 3	C101	A - 3	CN9	E - 1	IC37	C - 3	Q007	B - 1	R042	A - 3	R106	B - 1		
C008	A - 1	C102	B - 1	CN10	A - 2	IC38	C - 3	Q008	B - 1	R043	A - 3	R107	B - 2		
C009	A - 1	C103	B - 2	CN11	B - 2	IC39	D - 1	Q009	A - 2	R044	A - 1	R108	C - 1		
C010	A - 2	C104	A - 3	CN12	B - 2	IC40	D - 1	Q010	A - 2	R045	A - 1	R109	C - 2		
C011	A - 3	C105	A - 3			IC41	D - 1	Q011	A - 2	R046	B - 1	R110	C - 2		
C012	A - 3	C106	A - 3			IC42	D - 2	Q012	A - 1	R047	B - 1	R111	C - 2		
C013	A - 3	C107	A - 3			IC43	D - 2	Q013	A - 1	R048	B - 1	R112	C - 2		
C014	A - 1	C108	B - 3	D001	A - 2	IC44	D - 3	Q014	B - 1	R049	B - 1	R113	C - 2		
C015	A - 1	C109	B - 3	D002	A - 3	IC45	D - 3	Q015	B - 1	R050	B - 1	R114	C - 2		
C016	A - 3	C110	B - 3	D003	A - 2	IC46	D - 3	Q016	A - 2	R051	A - 1	R115	C - 3		
C017	A - 3	C111	B - 3	D004	B - 1	IC47	D - 1	Q017	A - 1	R052	A - 1	R116	C - 3		
C018	A - 1	C112	B - 3	D005	B - 1	IC48	E - 2	Q018	A - 2	R053	A - 1	R117	C - 3		
C019	A - 2	C113	B - 3	D006	B - 1	IC49	D - 2	Q019	A - 1	R054	A - 1	R118	C - 3		
C020	A - 1	C114	B - 3	D007	B - 1	IC50	D - 3	Q020	A - 3	R055	A - 1	R119	B - 2		
C021	A - 3	C115	B - 3			IC51	D - 3	Q021	A - 3	R056	B - 1	R120	C - 1		
C022	A - 3	C116	B - 3			IC52	D - 3	Q022	A - 3	R057	A - 1	R121	D - 1		
C023	A - 3	C117	B - 3			IC53	D - 3	Q023	A - 2	R058	A - 2	R122	D - 3		
C024	A - 3	C118	B - 3	DL1	A - 1	IC54	E - 1	Q024	A - 2	R059	A - 2	R123	E - 1		
C025	B - 1	C119	B - 3			IC55	E - 1	Q025	A - 2	R060	A - 3	R124	E - 2		
C026	A - 2	C120	B - 1			IC56	E - 1	Q026	C - 2	R061	A - 3	R125	E - 2		
C027	A - 2	C121	B - 1			IC57	E - 2	Q027	B - 1	R062	A - 3	R126	E - 3		
C028	A - 3	C122	C - 3	IB1	B - 2	IC58	E - 3	Q028	A - 2	R063	A - 3	R127	E - 3		
C029	B - 1	C123	B - 3	IB2	B - 2	IC59	E - 3			R064	A - 2	R128	E - 3		
C030	A - 1	C124	C - 3	IB3	D - 1	IC60	E - 3			R065	A - 3	R129	E - 1		
C031	A - 2	C125	C - 3	IB4	D - 1	IC61	E - 3			R066	A - 3	R130	E - 1		
C032	A - 2	C126	C - 1	IB5	E - 2	IC62	E - 1	R001	A - 1	R067	A - 2	R131	C - 1		
C033	A - 3	C127	C - 1	IB6	E - 2	IC63	E - 2	R002	A - 1	R068	A - 3	R132	B - 1		
C034	B - 1	C128	C - 1			IC64	E - 2	R003	A - 1	R069	B - 1	R133	E - 2		
C035	B - 1	C129	C - 2			IC65	E - 3	R004	A - 1	R070	B - 1	R134	E - 1		
C036	A - 2	C130	C - 3			IC66	E - 3	R005	A - 1	R071	B - 1	R135	A - 3		
C037	B - 1	C131	D - 3	IC1	A - 3	IC67	E - 3	R006	A - 1	R072	B - 1	R136	A - 3		
C038	B - 1	C132	D - 3	IC2	B - 3	IC68	E - 3	R007	A - 1	R073	B - 1				
C039	B - 1	C133	D - 1	IC3	B - 3			R008	A - 2	R074	A - 1				
C040	B - 2	C134	D - 2	IC4	B - 3			R009	A - 2	R075	A - 2				
C041	A - 2	C135	D - 2	IC5	B - 3			R010	A - 2	R076	A - 2	RY001	B - 1		
C042	A - 2	C136	D - 3	IC6	B - 3	JW1	B - 3	R011	A - 2	R077	A - 2				
C043	B - 1	C137	D - 3	IC7	A - 3	JW2	B - 3	R012	A - 2	R078	A - 2				
C044	B - 1	C138	D - 3	IC8	A - 3	JW3	C - 3	R013	A - 3	R080	B - 1				
C045	A - 2	C139	E - 1	IC9	B - 3	JW4	C - 3	R014	A - 3	R081	B - 1	VC1	A - 3		
C046	A - 2	C140	E - 1	IC10	B - 3	JW5	C - 2	R015	A - 1	R082	B - 1	VC2	A - 3		
C047	A - 2	C141	D - 1	IC11	B - 3	JW6	D - 3	R016	A - 1	R083	B - 1				
C048	A - 3	C142	E - 3	IC12	B - 3	JW7	D - 2	R017	A - 1	R084	B - 1				
C049	B - 1	C143	E - 3	IC13	A - 2	JW8	D - 2	R018	A - 1	R085	A - 1				
C050	B - 2	C144	E - 3	IC14	A - 2	JW9	E - 2	R019	A - 1	R086	A - 1	VR001	A - 1		
C051	C - 2	C145	E - 3	IC15	A - 3	JW10	E - 2	R020	A - 1	R087	A - 2	VR002	A - 1		
C052	B - 1	C146	E - 1	IC16	B - 2	JW11	D - 3	R021	A - 1	R088	A - 2	VR003	A - 1		
C053	C - 2	C147	E - 2	IC17	B - 2	JW12	E - 3	R022	A - 1	R089	B - 1	VR004	A - 2		
C054	C - 2	C148	E - 2	IC18	B - 1	JW13	E - 3	R023	A - 2	R090	B - 1				
C055	C - 2	C149	E - 3	IC19	B - 1	JW14	E - 3	R024	A - 1	R091	A - 1				
C056	C - 1	C150	E - 3	IC21	B - 2	JW15	E - 3	R025	A - 1	R092	B - 2				
C057	C - 2	C151	E - 3	IC22	B - 2			R026	A - 1	R093	A - 2	X1	A - 3		
C058	C - 2	C152	E - 3	IC23	B - 2			R027	A - 1	R094	A - 2				
C059	C - 2	C153	E - 3	IC24	B - 1			R028	A - 1	R095	A - 2				
C060	C - 2	C154	E - 3	IC25	C - 1	L001	A - 3	R029	A - 1	R096	A - 2				
C061	C - 2	C155	E - 3	IC26	C - 1	L002	A - 3	R030	A - 1	R097	B - 1				
C062	C - 3	C156	E - 3	IC27	C - 1	L003	A - 2	R031	A - 1	R098	B - 1				
C063	C - 3			IC28	C - 1	L004	A - 2	R032	A - 1	R099	A - 1				
C064	C - 3			IC29	C - 2	L005	B - 1	R033	A - 2						
C065	D - 3			IC30	C - 2	L006	B - 1	R034	A - 2						
								R035	A - 2						

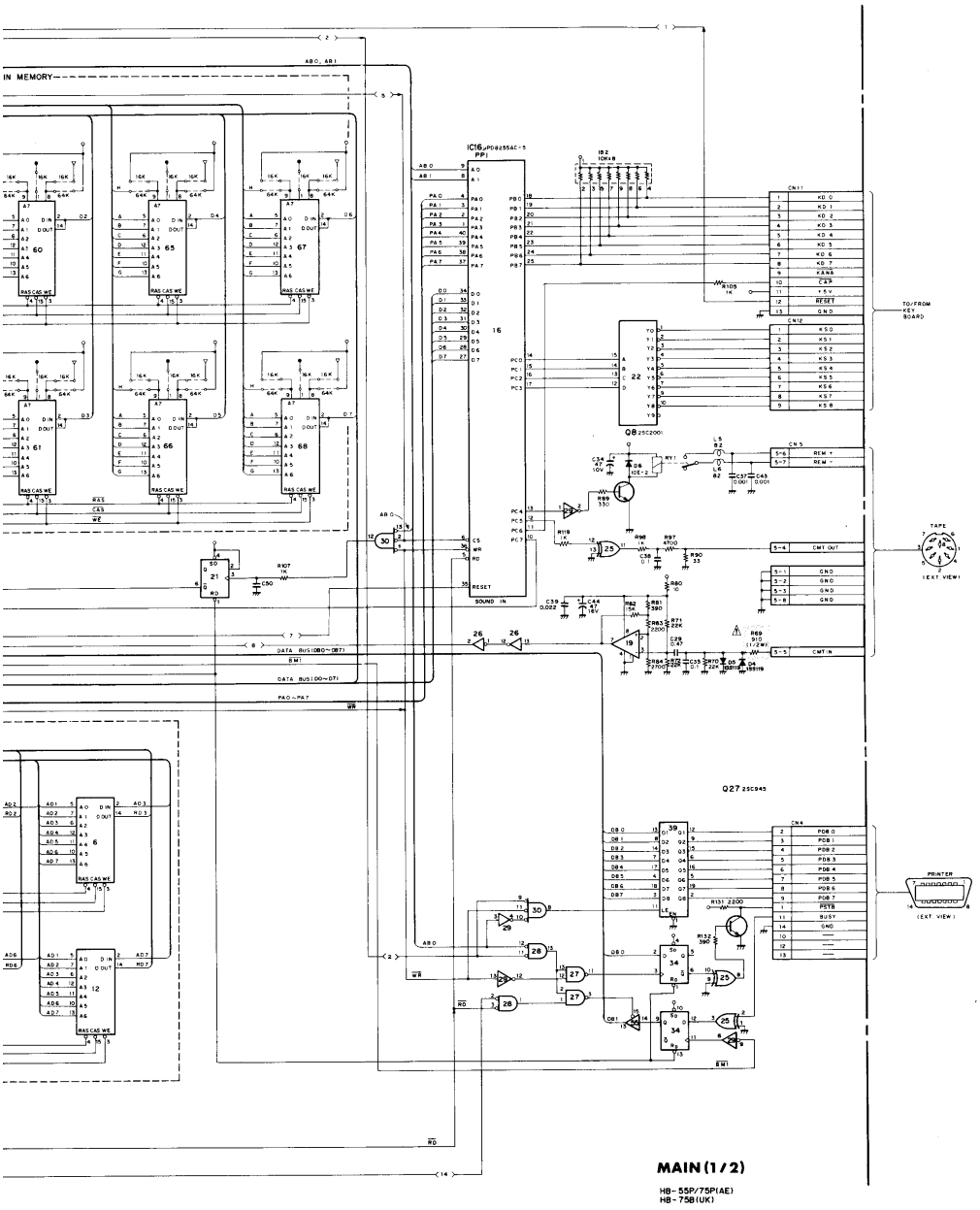
MAIN(1/2)



/2) MAIN(1/2)

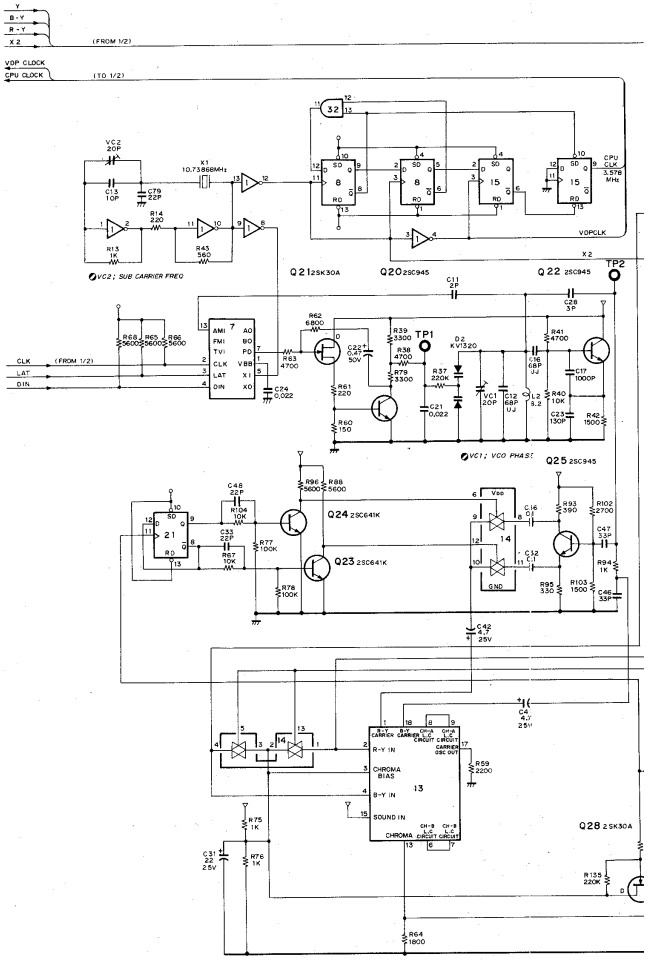

IC48 AY-3-8910 PSG
BASIC ROM
FIRM WARE
Q26 2SC945
RESET
CLK
DATA BUS (D0~D7)
CONTROL BUS
ADDRESS BUS
SOUND IN
TRG1 A
TRG2 A
TRG1 B
TRG2 B
OUT A
OUT B
FWD A
BACK A
LEFT A
RIGHT A
FWD B
BACK B
LEFT B
RIGHT B
NOTE1(1/3)
NOTE2(1/1)
NOTE3(1/1)
NOTE4(1/1)

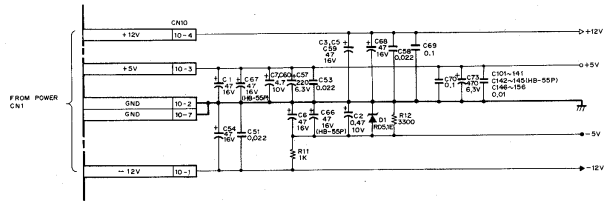

MAIN MEMORY
V-RAM
IC2 TMS9928ANL
VDP
NOTE 1 (2/3)
NOTE 1 (3/3)
CN8
CN9
AUDIO OUT R
AUDIO OUT L
RESET
CLK
WR
RD
INT
MODE
VDP CLOCK
RAS
CAS
R/W
DATA BUS (D0 ~ D7)
CONTROL BUS
PA0 ~ PA7
ABO ~ AB15

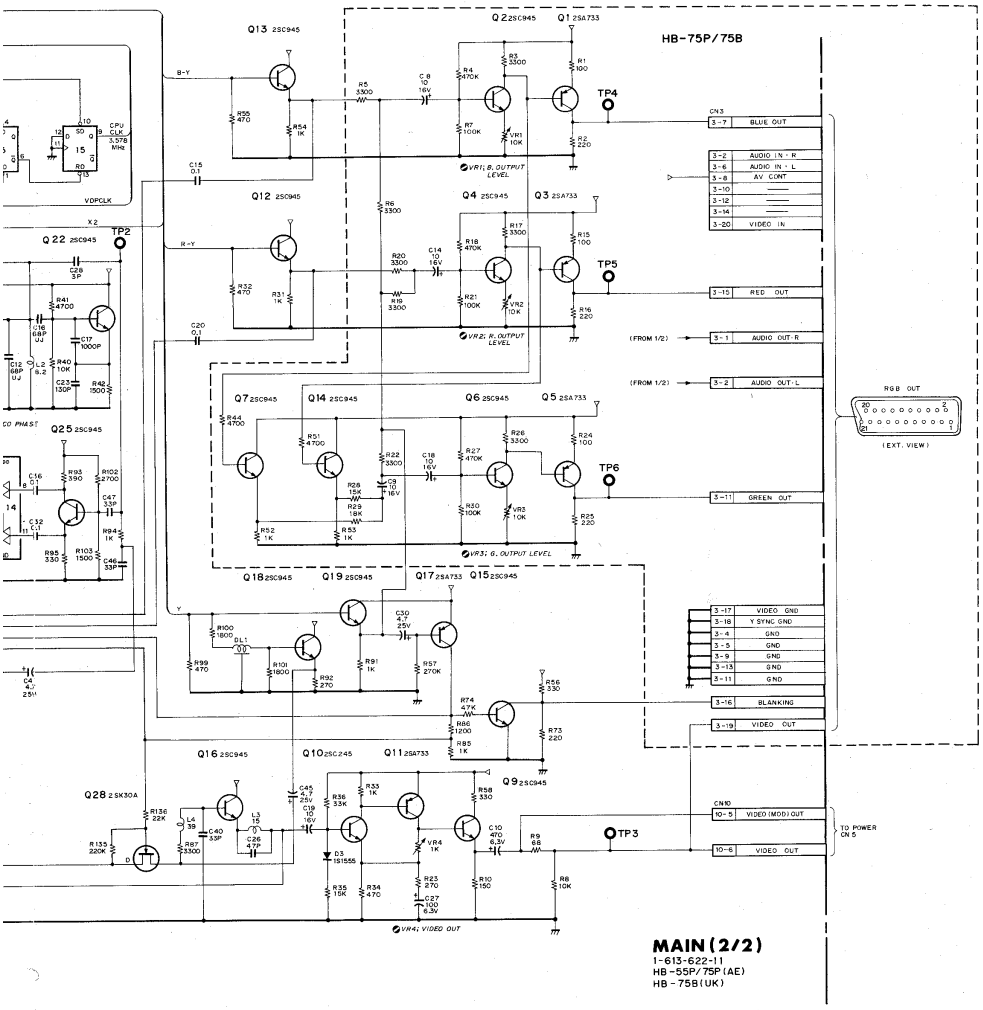

IN MEMORY
IC16 μPD8255AC-5 PPI
Q8 2SC2001
Q27 2SC945
CN11
CN12
CN3
CN4
TO/FROM KEY BOARD
TAPE
PRINTER
(EXT VIEW)
SOUND IN
DATA BUS(D0~D7)
PA0~PA7
MAIN(1/2)
HB-55P/75P(AE)
HB-75B(UK)

MAIN(2/2)

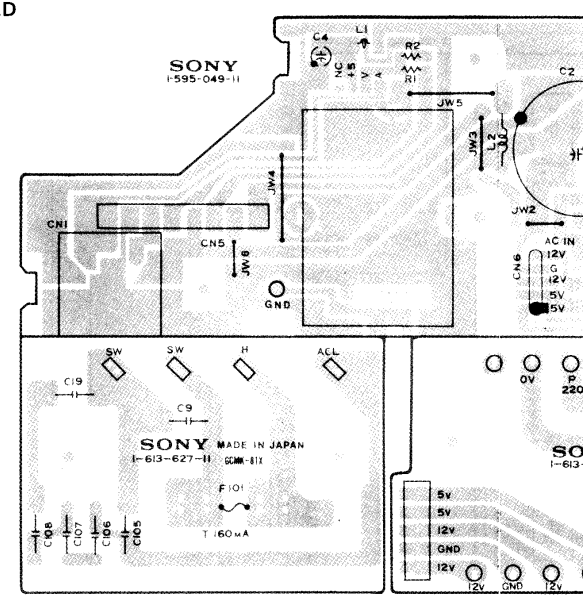
REF.NO.	TYPE NO.	PIN NO.			
		+12V	+5 V	GND	-5 V
IC1	SN74LS04N,MB74LS04		14	7	
IC2	TMS9929ANL		33	12	
IC3	MCM4116BP20,UPD416C-2	8	9	16	1
IC4	MCM4116BP20,UPD416C-2	8	9	16	1
IC5	MCM4116BP20,UPD416C-2	8	9	16	1
IC6	MCM4116BP20,UPD416C-2	8	9	16	1
IC7	CX7925A-1,CX7925A		12	14	
IC8	SN74LS74AN,MB74LS74A		14	7	
IC9	MCM4116BP20,UPD416C-2	8	9	16	1
IC10	MCM4116BP20,UPD416C-2	8	9	16	1
IC11	MCM4116BP20,UPD416C-2	8	9	16	1
IC12	MCM4116BP20,UPD416C-2	8	9	16	1
IC13	LM1889N				
IC14	uPD4066BC,HD14066BP	14		7	
IC15	SN74LS74AN,MB74LS74A		14	7	
IC16	uPD8255AC-5		26	7	
IC17	SN74LS153N,MB74LS153		16	8	
IC18	SN74LS139N,MB74LS139		16	8	
IC19	uPC311C		8	1	
IC20	----------				
IC21	SN74LS74AN,MB74LS74A		14	7	
IC22	SN74LS145N,MB74LS145		16	8	
IC23	SN74LS139N,MB74LS139		16	8	
IC24	SN74LS32N,MB74LS32		14	7	
IC25	SN74LS86N,HD74LS86P		14	7	
IC26	SN74LS04N,MB74LS04		14	7	
IC27	SN74LS00N,MB74LS00		14	7	
IC28	SN74LS02N,MB74LS02		14	7	
IC29	SN74LS04N,MB74LS04		14	7	
IC30	SN74LS27N,MB74LS27		14	7	
IC31	SN74LS175N,MB74LS175		16	8	
IC32	SN74LS08N,MB74LS08		14	7	
IC33	SN74LS126AN,		14	7	
IC34	SN74LS74AN,MB74LS74A		14	7	
IC35	SN74LS74AN,MB74LS74A		14	7	
IC36	SN74LS11N,MB74LS11		14	7	
IC37	SN74LS08N,MB74LS08		14	7	
IC38	SN74LS04N,MB74LS04		14	7	
IC39	SN74LS373N,MB74LS373		20	10	
IC40	SN74LS645N,MB74LS645		20	10	
IC41	LH0080A,UPD780C-1		11	29	
IC42	MSM38256-70RS		28	14	
IC43					
IC44	MSM38128A-77RS		28	14	
IC45	SN74LS10N,MB74LS10		14	7	
IC46	SN74LS32N,MB74LS32		14	7	
IC47	SN74LS367AN,MB74LS367A		16	8	
IC48	AY-3-8910,YM2149		40	1	
IC49	SN74LS157N,MB74LS157		16	8	
IC50	SN74LS74AN,MB74LS74A		14	7	
IC51	SN74LS74AN,MB74LS74A		14	7	
IC52	SN74LS02N,MB74LS02		14	7	
IC53	SN74LS27N,MB74LS27		14	7	
IC54	SN74LS367AN,MB74LS367A		16	8	
IC55	SN74LS367AN,MB74LS367A		16	8	
IC56	SN74LS367AN,MB74LS367A		16	8	
IC57	SN74LS157N,MB74LS157		16	8	
IC58	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	
IC59	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	
IC60	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	
IC61	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	
IC62	SN74LS157N,MB74LS157		16	8	
IC63	SN74LS157N,MB74LS157		16	8	
IC64	SN74LS09N,MB74LS09		14	7	
IC65	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	
IC66	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	
IC67	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	
IC68	uPD416C-2 (HB-55P)	8	9	16	1
	MSM3764-15RS(HB-75P/75B)		8	16	






HB-75P/75B
MAIN (2/2)
1-613-622-11
HB-55P/75P(AE)
HB-75B(UK)
TP2
TP3
TP4
TP5
TP6
CN3
CN10
BLUE OUT
AUDIO IN - R
AUDIO IN - L
AV CONT
VIDEO IN
RED OUT
AUDIO OUT-R
AUDIO OUT-L
GREEN OUT
VIDEO GND
Y SYNC GND
GND
BLANKING
VIDEO OUT
VIDEO (MOD) OUT
TO POWER CN5
RGB OUT
(EXT. VIEW)
(FROM 1/2)
VR1; B. OUTPUT LEVEL
VR2; R. OUTPUT LEVEL
VR3; G. OUTPUT LEVEL
VR4; VIDEO OUT

FUSE, LED, POWER, TRANS, 5V, 12V BOARD

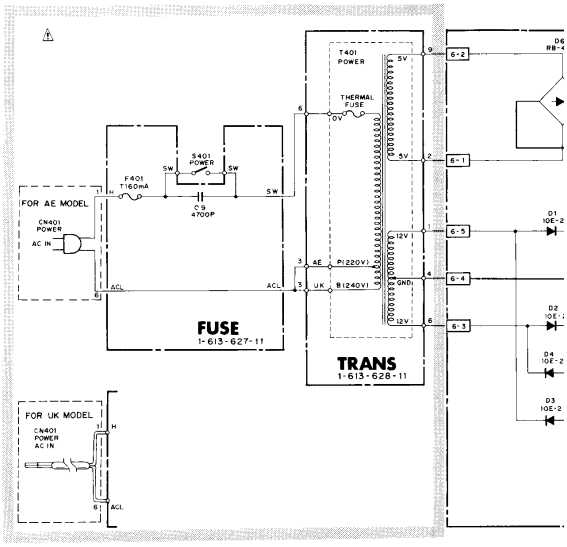


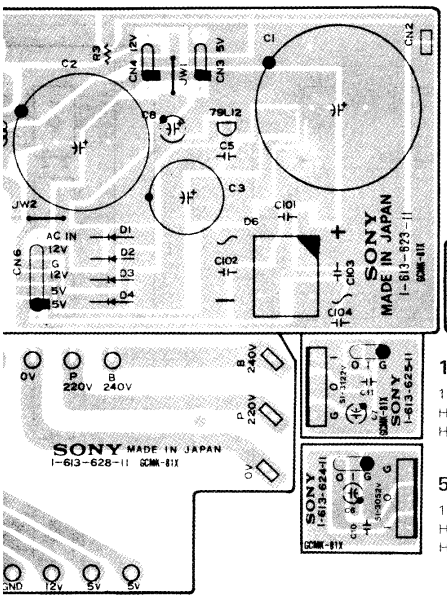
FUSE – COMPONENT SIDE –

1-613-627-11
HB-55P/75P(AE)
HB-75B(UK)

TRANS – COMPO

1-613-628-11
HB-55P/75P(AE)
HB-75B(UK)





POWER – COMPONENT SIDE –

1-613-623-11
HB-55P/75P(AE)
HB-75B(UK)

LED – COMPONENT SIDE –

1-613-626-11
HB-55P/75P(AE)
HB-75B(UK)

12V – COMPONENT SIDE –

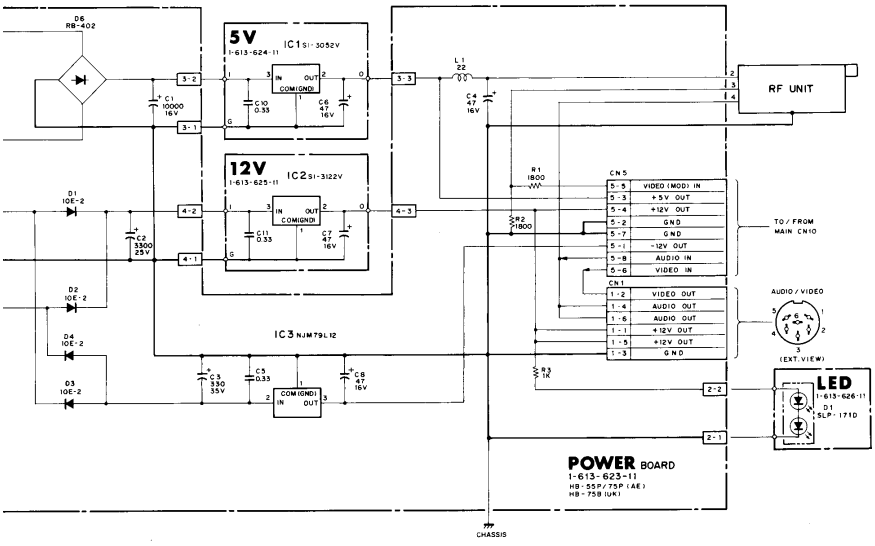
1-613-625-11
HB-55P/75P(AE)
HB-75B(UK)

5V – COMPONENT SIDE –

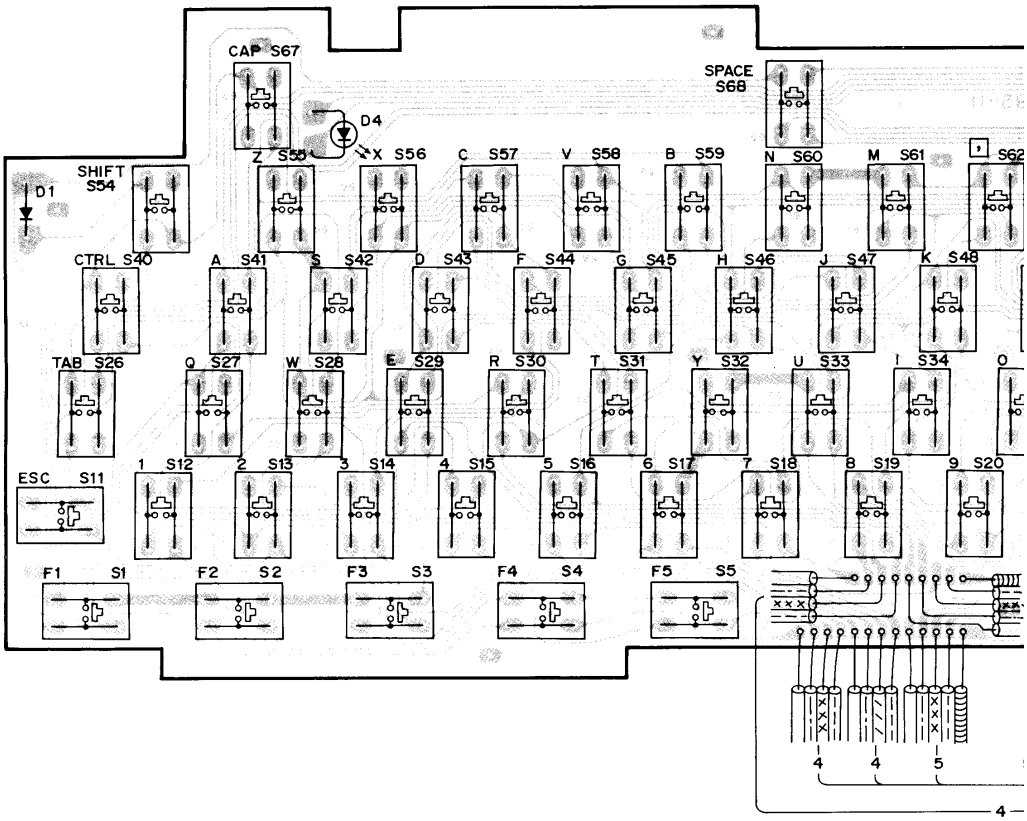
1-613-624-11
HB-55P/75P(AE)
HB-75B(UK)

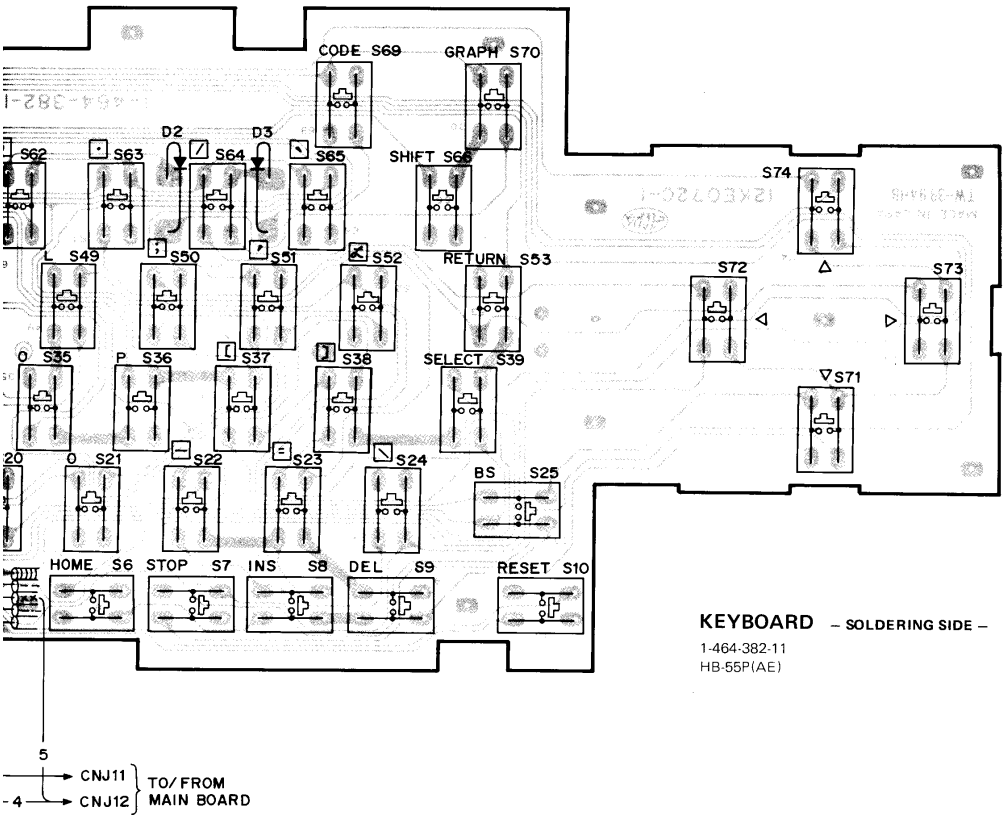
– COMPONENT SIDE –

-11
5P(AE)
K)



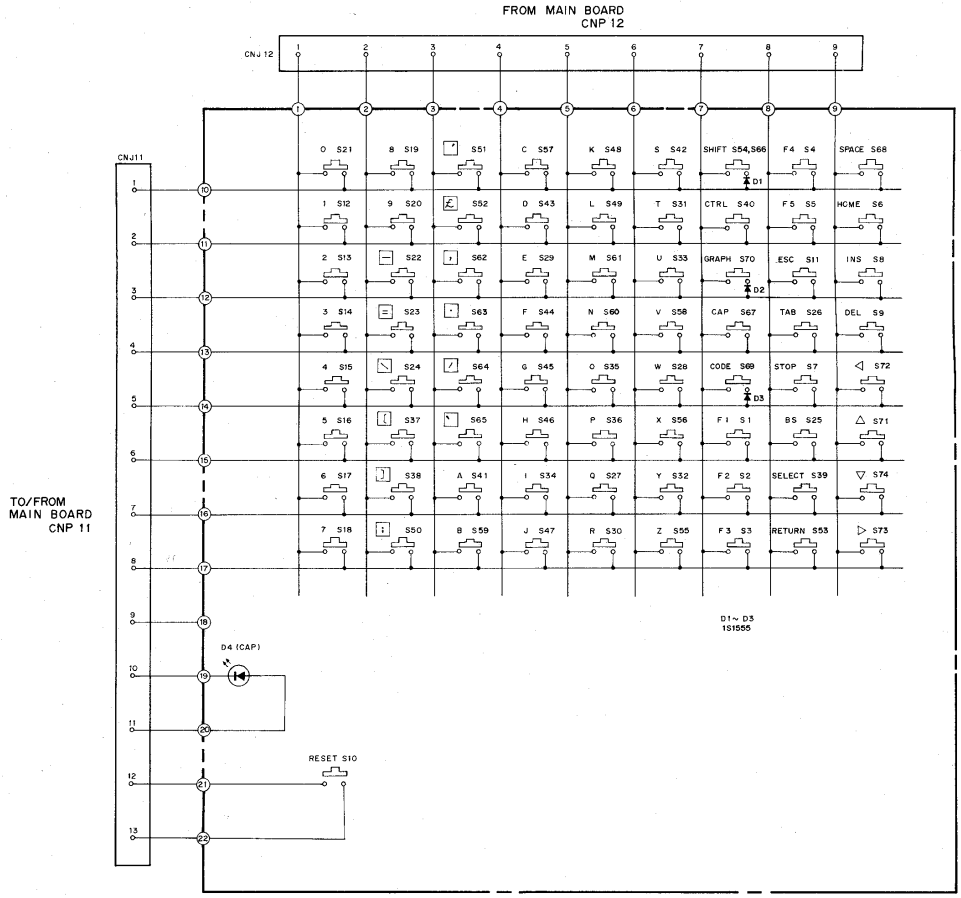
KEYBOARD (HB-55P)





KEYBOARD – SOLDERING SIDE –

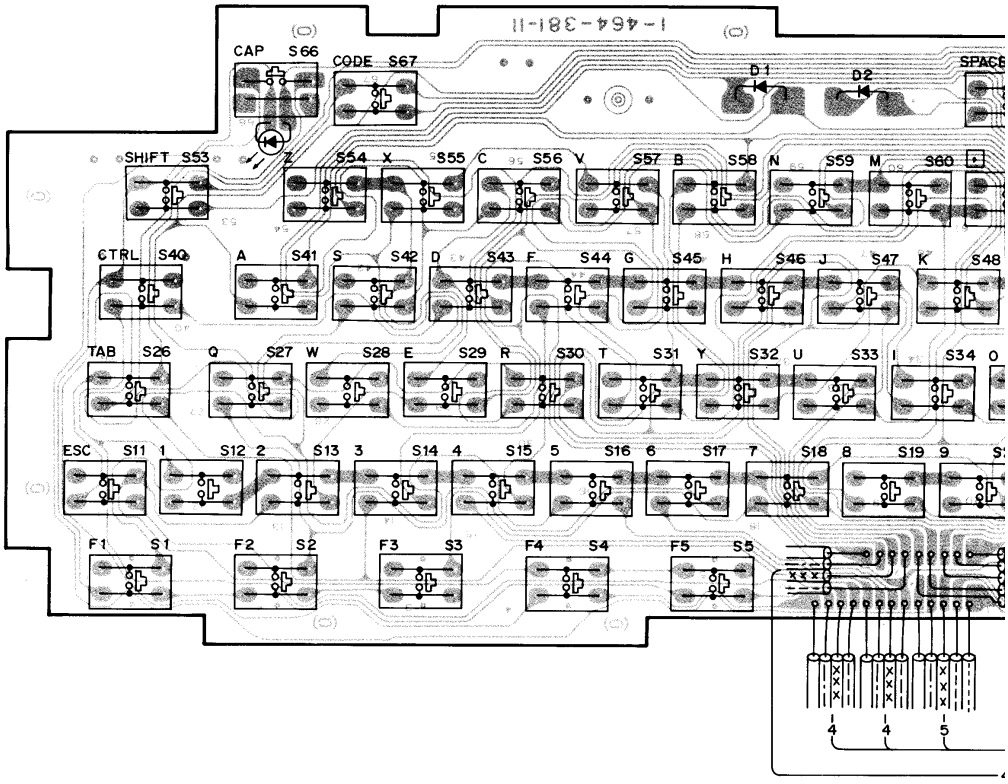
1-464-382-11
HB-55P(AE)

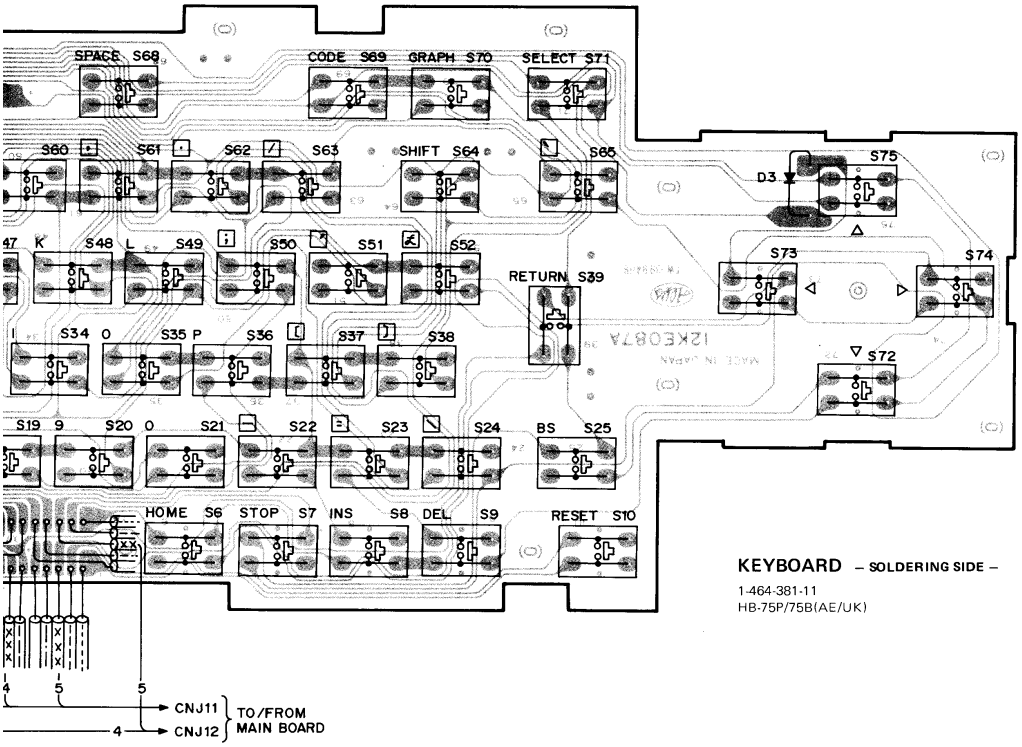


KEY

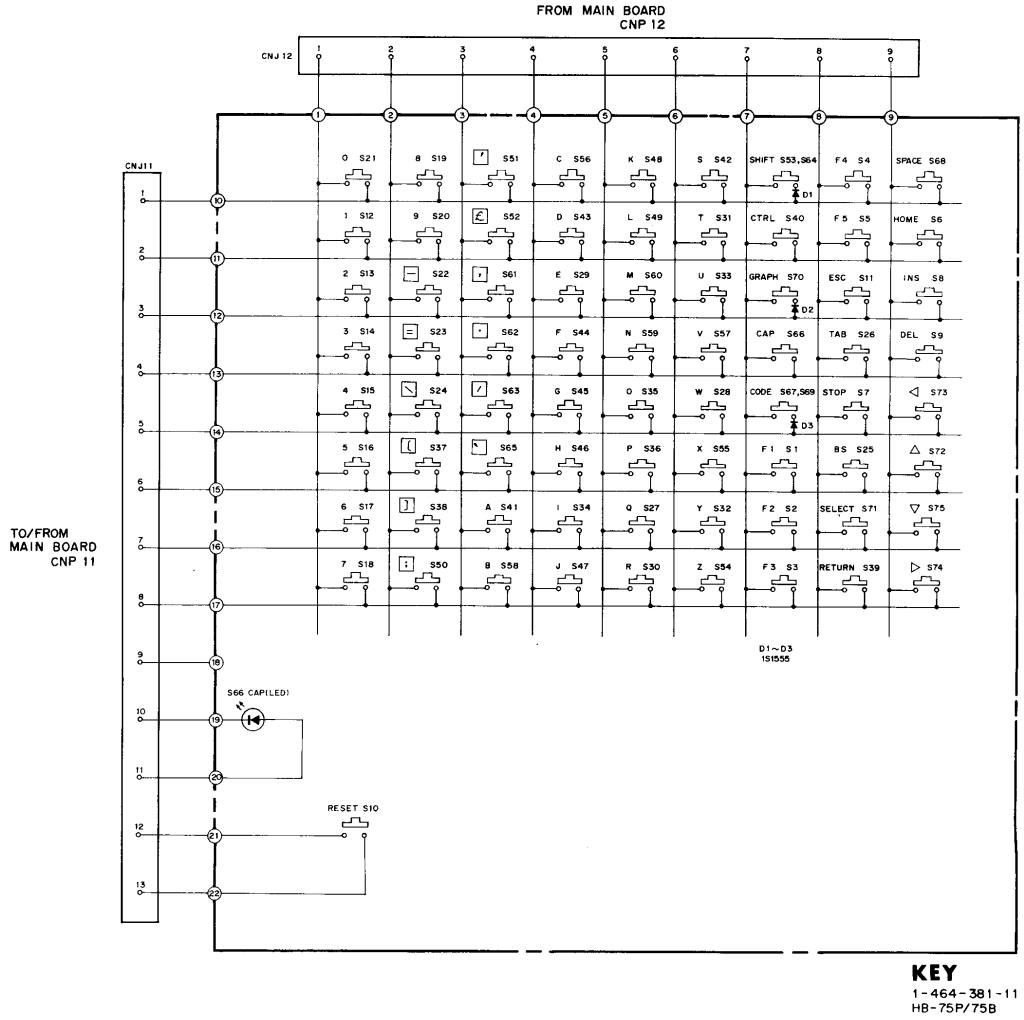
1-464-382-11
HB-55P

KEYBOARD (HB-75P/75B)





KEYBOARD – SOLDERING SIDE –
1-464-381-11
HB-75P/75B(AE/UK)



KEY

1-464-381-11
HB-75P/75B

CHAPTER 6
ALIGNMENT

6-1. HB-55P/75P/75B ADJUSTMENT

Note: Adjustment should be performed in the order mentioned below.

6-1-1. VCO Phase Adjustment

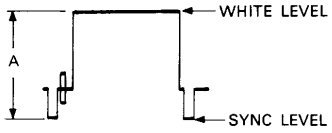
Equipment Required: Digital Volt Meter
Check Point : TP1 (Junction Point of R37 and R38)/ MAIN
Specification : 7.0V ± 0.1V
Adjustment : VC1/MAIN

6-1-2. SUB Carrier Frequency Adjustment

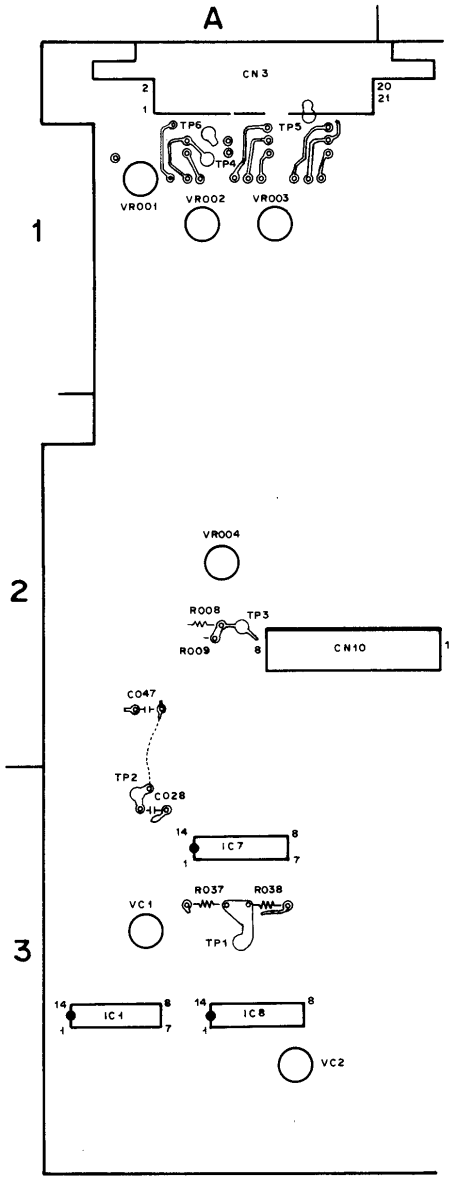
Equipment Required: FREQUENCY COUNTER
Check Point : TP2 (Junction Point of C28 and C47)/ MAIN
Specification : 4.433618 MHz ± 10 Hz
Adjustment : VC2/MAIN

6-1-3. Video Output Level Adjustment

Equipment Required: OSCILLOSCOPE
Condition : ① Terminated pin 2 of CN1 (AUDIO/ VIDEO OUTPUT)/POWER between GND with 75Ω, or connect the Monitor TV (75Ω INPUT) to CN1/ POWER. But, do not connect to CN3 (RGB OUTPUT)/MAIN.
② Example
BASIC will have the list programmed and run.
10 COLOR␣15, 15
20 END
Check Point : TP3 (pin 2 of CN1)/POWER
Specification : A = 1V ± 0.1 Vp-p



Adjustment : VR4/MAIN



MAIN BOARD
– COMPONENT SIDE –

6-2. HB-75P/75B RGB ADJUSTMENT

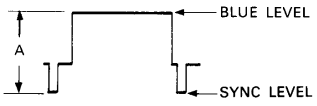
Note 1: After adjusting step 6-1, the following adjustment should be performed.

Note 2: Adjustment should be performed by terminating each test point between GND with 75Ω or , connect the Monitor TV (75Ω INPUT) to CN3 (RGB OUTPUT)/MAIN. But do not connect to CN1 (AUDIO/VIDEO OUTPUT)/ POWER.

Note 3: Example
BASIC will have the list programmed and run
10 COLOR _, 15, 15
20 END

6-2-1. Blue Output Level Adjustment

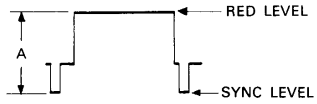
Equipment Required: OSCILLOSCOPE
Check Point : TP4 (pin 3 of CN3 or collector of Q1)/MAIN
Specification : A = 0.7V ± 0.1 Vp-p



Adjustment : VR1/MAIN

6-2-2. Red Output Level Adjustment

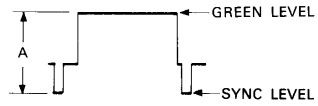
Equipment Required: OSCILLOSCOPE
Check Point : TP5 (pin 15 of CN3 or collector of Q3)/MAIN
Specification : A = 0.7V ± 0.1 Vp-p



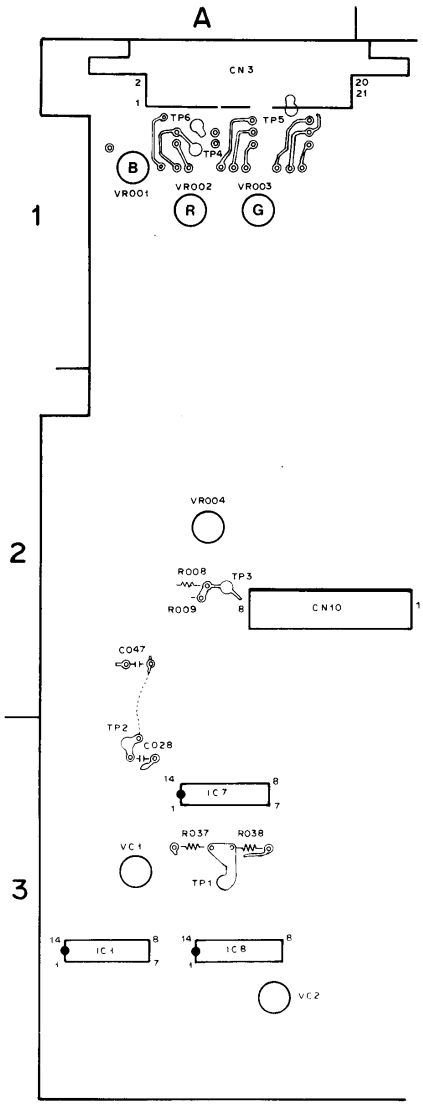
Adjustment : VR2/MAIN

6-2-3. Green Output Level Adjustment

Equipment Required: OSCILLOSCOPE
Check Point : TP6 (pin 11 of CN3 or collector of Q5)/MAIN
Specification : A = 0.7V ± 0.1 Vp-p



Adjustment : VR3/MAIN



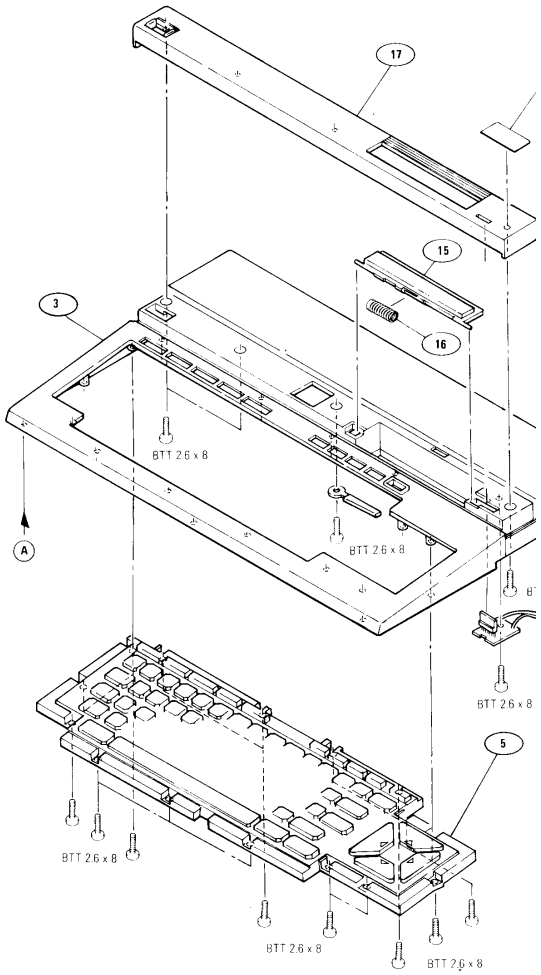
MAIN BOARD
– COMPONENT SIDE –

CHAPTER 7
REPAIR PARTS AND FIXTURE

7-1. EXPLODED VIEW

MAIN ASSEMBLY (HB-55P)

No.	Part No.	Description
⚠ 1	A-8050-100-A	MOUNTED CB, MAIN
2	A-8050-102-A	MOUNTED CB, POWER (WITH 5V, 12V BOARD)
3	X-4604-316-1	CABINET (UPPER) ASSY
⚠ 4	**1-447-939-11**	**TRANSFORMER, POWER**
5	1-464-382-11	KEYBOARD UNIT
⚠ 6	**1-534-817-XX**	**CORD, POWER, EULO PLUG**
⚠ 7	**1-553-318-00**	**SWITCH, PUSH (AC POWER)(1 KEY)**
8	1-613-624-11	PC BOARD, 5V
9	1-613-625-11	PC BOARD, 12V
10	1-613-627-11	PC BOARD, FUSE
11	1-613-628-11	PC BOARD, TRANSFORMER
⚠ 12	**3-703-244-00**	**BUSHING, CORD**
13	**3-706-165-00**	**SCREW**
14	**4-604-301-00**	**BUTTON, POWER SWITCH**
15	**4-604-302-00**	**LID, CARTRIDGE**
16	**4-604-303-00**	**SPRING**
17	**4-604-306-31**	**PLATE, ORNAMENTAL**
18	**4-604-332-01**	**LABEL, CONTROL**
19	4-604-335-01	PLATE, BLIND (A)
20	4-604-337-01	PLATE, BLIND (C)
21	4-604-386-01	COVER, CARTRIDGE
22	4-604-394-02	PLATE, BOTTOM
23	4-605-103-01	LABEL, CAUTION
24	4-605-131-01	INSULATOR, FUSE, PC BOARD
25	4-605-132-01	INSULATOR, TRANSFORMER PCB
26	**4-812-134-11**	**RIVET NYLON, 3.5**
27	**4-860-711-00**	**FELT**
28	**4-864-307-00**	**RING**
29	**4-875-726-00**	**SHEET, INSULATING**
30	**4-886-557-00**	**CLIP (B), IC**
31	**4-886-865-00**	**CUSHION (A)**



NOTE:

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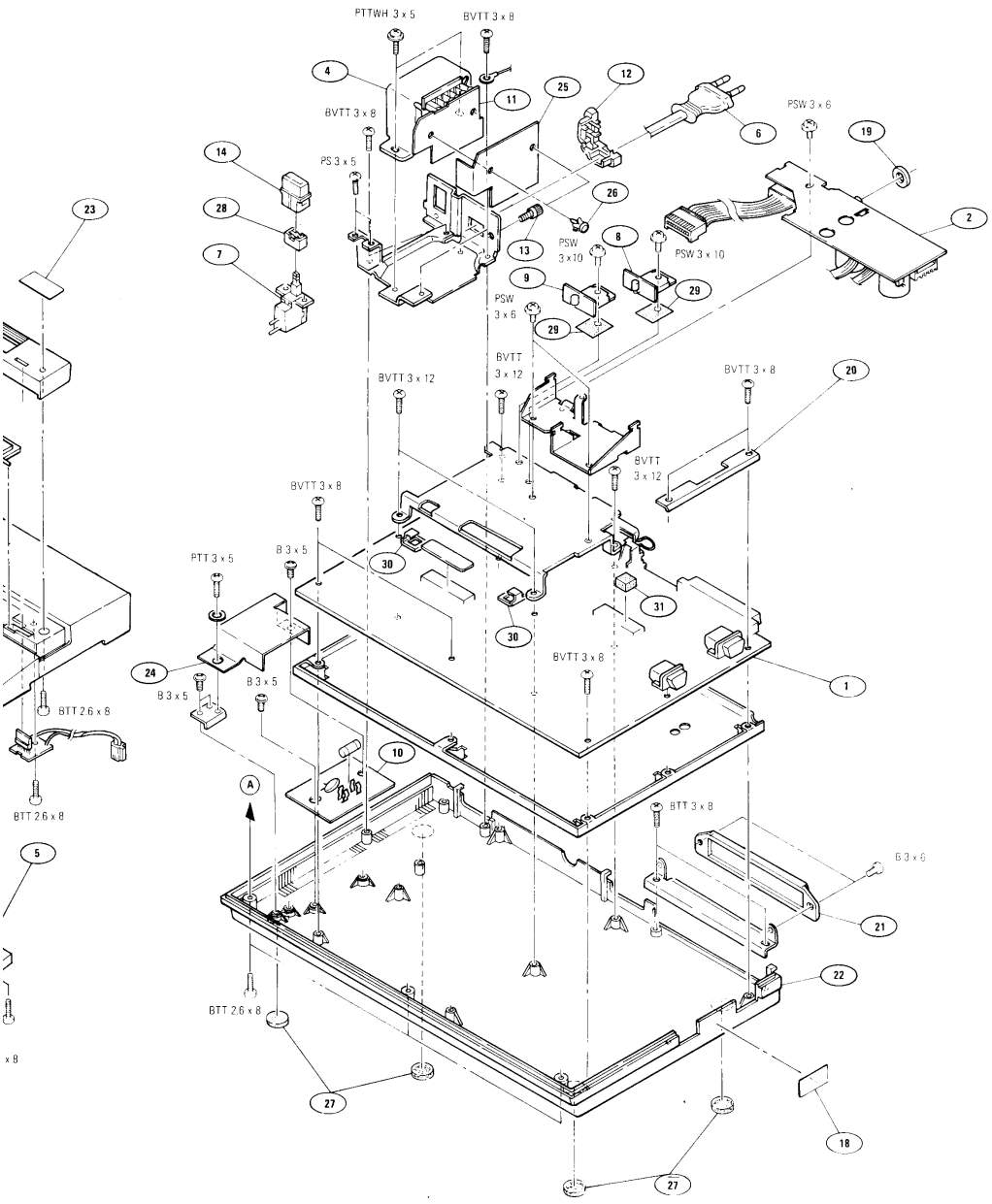
2. Parts printed in Bold-Face type are normally stocked for replacement purposes. The remaining parts shown in this manual are not normally required for routine service work. Orders for parts not shown in Bold-Face type will be processed, but allow for additional delivery time.
3. Item with no part number and/or no description are not stocked because they are seldom required for routine service.


PTTWH 3 x 5
BVTT 3 x 8
BVTT 3 x 8
PS 3 x 5
PSW 3 x 6
PSW 3 x 10
PSW 3x10
PSW 3 x 6
BVTT 3 x 12
BVTT 3 x 12
BVTT 3 x 8
BVTT 3 x 8
BVTT 3 x 12
PTT 3 x 5
B 3 x 5
B 3 x 5
B 3 x 5
BTT 2.6 x 8
BTT 2.6 x 8
BTT 3 x 8
B 3 x 6
BTT 2.6 x 8
A
1
2
4
5
6
7
8
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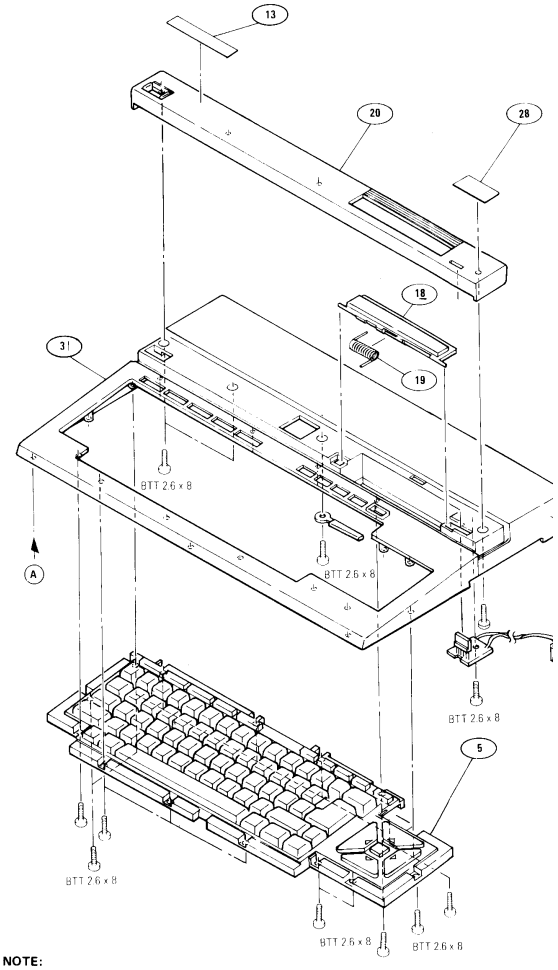
MAIN ASSEMBLY (HB-75P/75B)

No.	Part No.	Description
⚠ 1	A-8050-098-A	MOUNTED CB, MAIN
2	A-8050-102-A	MOUNTED CB, POWER (75P) (WITH 5V, 12V BOARD)
	A-8050-103-A	MOUNTED CB, POWER (75B) (WITH 5V, 12V BOARD)
3	X-4604-313-1	CABINET (UPPER) ASSY (75B)
	X-4604-314-1	CABINET (UPPER) ASSY (75P)
⚠ **4**	**1-447-939-11**	**TRANSFORMER, POWER**
5	1-464-381-11	KEYBOARD UNIT
⚠ **6**	**1-534-817-XX**	**CORD POWER, EULO PLUG (75P)**
⚠ **7**	**1-551-884-00**	**CORD, POWER (75B)**
⚠ **8**	**1-553-318-00**	**SWITCH, PUSH (AC POWER)**
9	1-613-624-11	PC BOARD, 5V
10	1-613-625-11	PC BOARD, 12V
11	1-613-627-11	PC BOARD, FUSE
12	1-613-628-11	PC BOARD, TRANS
13	**3-701-690-00**	**LABEL (MADE IN JAPAN) (75B)**
14	**3-703-082-21**	**LABEL, CAUTION (75B)**
⚠ **15**	**3-703-244-00**	**BUSHING, CORD**
16	**3-706-165-00**	**SCREW**
17	**4-604-301-00**	**BUTTON, POWER SWITCH**
18	**4-604-302-00**	**LID, CARTRIDGE**
19	**4-604-303-00**	**SPRING**
20	**4-604-306-41**	**PLATE, ORNAMENTAL (75P)**
	4-604-306-51	**PLATE, ORNAMENTAL (75B)**
21	**4-604-332-01**	**LABEL, CONTROL**
22	4-604-335-01	PLATE, BLIND (A)
23	4-604-337-01	PLATE, BLIND (C)
24	4-604-355-01	REINFORCEMENT
25	4-604-356-02	CUSHION, RUBBER
26	4-604-382-02	PLATE, BOTTOM
27	4-604-386-01	COVER, CARTRIDGE
28	4-605-103-01	LABEL, CAUTION
29	4-605-131-01	INSULATOR, FUSE PC BOARD
30	4-605-132-01	INSULATOR, TRANSFORMER PCB
31	**4-812-134-11**	**RIVET NYLON, 3.5**
32	**4-860-711-00**	**FELT**
33	**4-864-307-00**	**RING**
34	**4-875-726-00**	**SHEET, INSULATING**
35	**4-886-557-00**	**CLIP (B), IC**
36	**4-886-865-00**	**CUSHION (A)**



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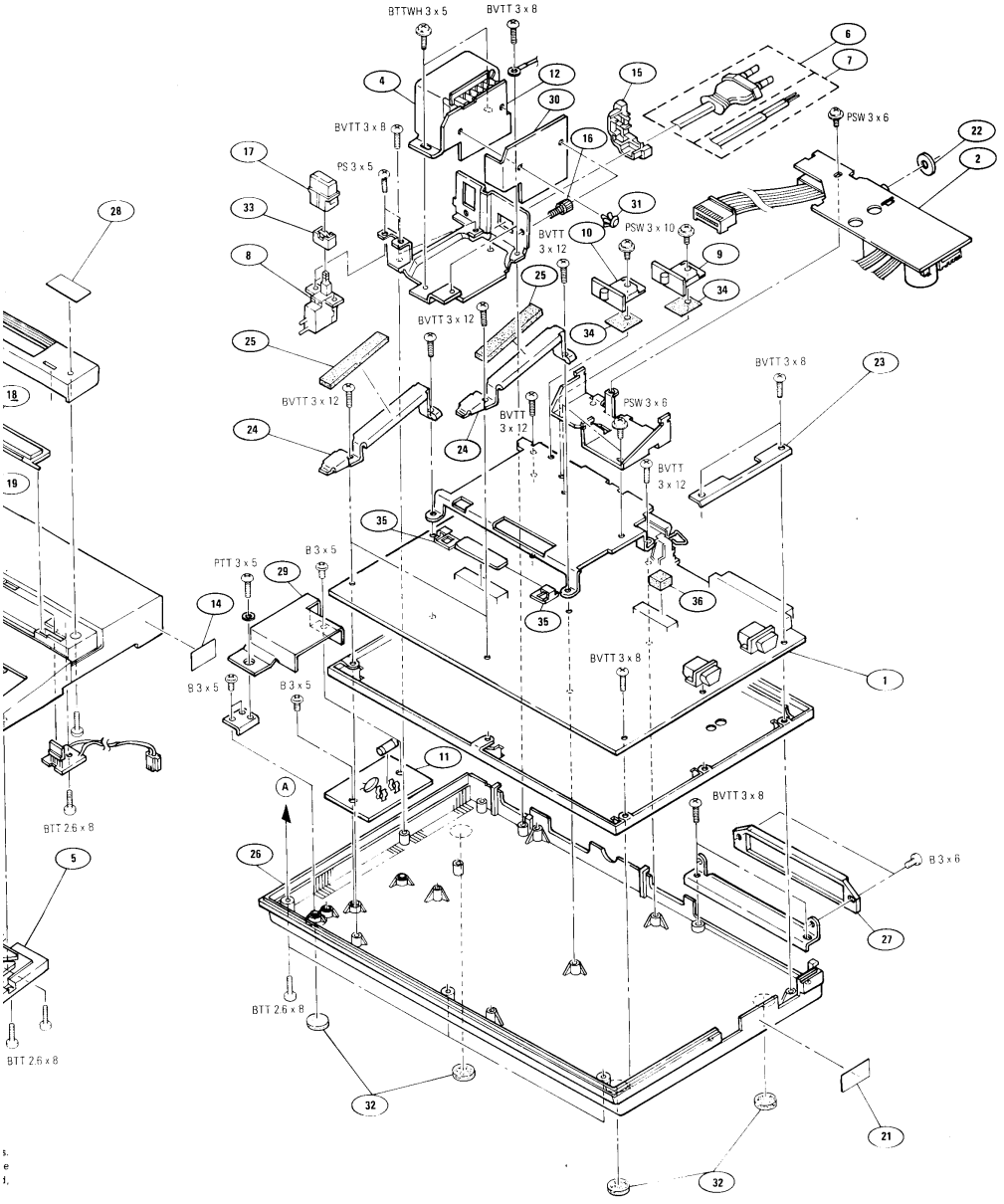
BTTWH 3 x 5
BVTT 3 x 8
PSW 3 x 6
PS 3 x 5
PSW 3 x 10
BVTT 3 x 12
PTT 3 x 5
B 3 x 5
BTT 2.6 x 8
B 3 x 6
A

KEYBOARD (HB-55P)

No.	Parts No.	Description
50	**9-983-716-01**	**KEY TOP (1) F1**
51	**9-983-717-01**	**KEY TOP (1) F2**
52	**9-983-718-01**	**KEY TOP (1) F3**
53	**9-983-719-01**	**KEY TOP (1) F4**
54	**9-983-720-01**	**KEY TOP (1) F5**
55	**9-983-721-01**	**KEY TOP (2) HOME**
56	**9-983-722-01**	**KEY TOP (2) STOP**
57	**9-983-723-01**	**KEY TOP (2) INS**
58	**9-983-724-01**	**KEY TOP (2) DEL**
59	**9-983-725-01**	**KEY TOP (2) RESET**
60	**9-983-726-01**	**KEY TOP (3) ESC**
61	**9-983-727-01**	**KEY TOP (4) CTRL**
62	**9-983-728-01**	**KEY TOP (5) CAP**
63	**9-983-729-01**	**KEY TOP (4) SHIFT**
64	**9-983-730-01**	**KEY TOP (4) TAB**
65	**9-983-731-01**	**KEY TOP (4) BS**
66	**9-983-733-01**	**KEY TOP (4) RETURN**
67	**9-983-735-01**	**KEY TOP (4) SELECT**
68	**9-985-313-01**	**KEY TOP (4) CODE**
69	**9-983-734-01**	**KEY TOP (4) GRAPH**
70	**9-985-264-01**	**KEY TOP (3) 1**
71	**9-985-265-01**	**KEY TOP (3) 2**
72	**9-985-266-01**	**KEY TOP (3) 3**
73	**9-985-267-01**	**KEY TOP (3) 4**
74	**9-985-268-01**	**KEY TOP (3) 5**
75	**9-985-269-01**	**KEY TOP (3) 6**
76	**9-985-270-01**	**KEY TOP (3) 7**
77	**9-985-271-01**	**KEY TOP (3) 8**
78	**9-985-272-01**	**KEY TOP (3) 9**
79	**9-985-273-01**	**KEY TOP (3) 0**
80	**9-985-274-01**	**KEY TOP (3) —**
81	**9-985-275-01**	**KEY TOP (3) =**
82	**9-985-276-01**	**KEY TOP (3) **
83	**9-985-277-01**	**KEY TOP (3) Q**
84	**9-985-278-01**	**KEY TOP (3) W**
85	**9-985-279-01**	**KEY TOP (3) E**
86	**9-985-280-01**	**KEY TOP (3) R**
87	**9-985-281-01**	**KEY TOP (3) T**
88	**9-985-282-01**	**KEY TOP (3) Y**
89	**9-985-283-01**	**KEY TOP (3) U**
90	**9-985-284-01**	**KEY TOP (3) I**
91	**9-985-285-01**	**KEY TOP (3) O**
92	**9-985-286-01**	**KEY TOP (3) P**
93	**9-985-287-01**	**KEY TOP (3) [**
94	**9-985-288-01**	**KEY TOP (3)]**
95	**9-985-289-01**	**KEY TOP (3) A**
96	**9-985-290-01**	**KEY TOP (3) S**
97	**9-985-291-01**	**KEY TOP (3) D**
98	**9-985-292-01**	**KEY TOP (3) F**
99	**9-985-293-01**	**KEY TOP (3) G**
100	**9-985-294-01**	**KEY TOP (3) H**
101	**9-985-295-01**	**KEY TOP (3) J**
102	**9-985-296-01**	**KEY TOP (3) K**
103	**9-985-297-01**	**KEY TOP (3) L**
104	**9-985-298-01**	**KEY TOP (3) ;**
105	**9-985-299-01**	**KEY TOP (3) '**
106	**9-985-300-01**	**KEY TOP (3) £**
107	**9-985-301-01**	**KEY TOP (3) Z**
108	**9-985-302-01**	**KEY TOP (3) X**
109	**9-985-303-01**	**KEY TOP (3) C**
110	**9-985-304-01**	**KEY TOP (3) V**
111	**9-985-305-01**	**KEY TOP (3) B**
112	**9-985-306-01**	**KEY TOP (3) N**
113	**9-985-307-01**	**KEY TOP (3) M**
114	**9-985-308-01**	**KEY TOP (3) ,**
115	**9-985-309-01**	**KEY TOP (3) .**
116	**9-985-310-01**	**KEY TOP (3) /**
117	**9-985-311-01**	**KEY TOP (3)**
118	**9-983-784-01**	**KEY TOP (6) SPACE**
119	**9-983-785-01**	**KEY TOP (7) CURSOR**
120	9-983-786-01	SPACE BAR
121	9-983-787-01	CURSOR BAR
122	**9-983-788-01**	**FRAME, KEYBOARD**
123	9-983-789-01	BAR HOLDER
124	**4-605-117-01**	**SPRING**

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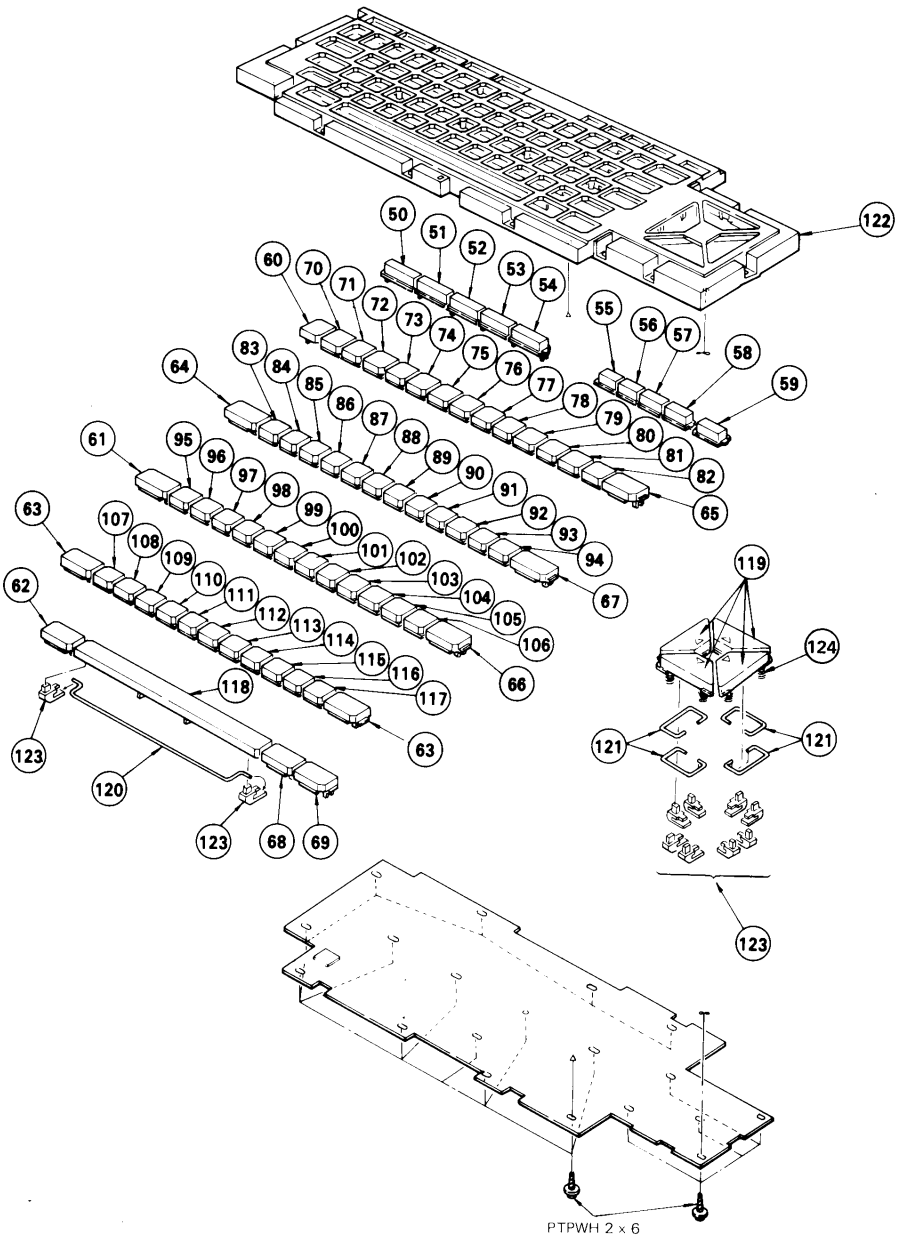
PTPWH 2 x 6

KEYBOARD (HB-75P/75B)

No.	Parts No.	Description
50	**9-983-716-01**	**KEY TOP (1) F1**
51	**9-983-717-01**	**KEY TOP (1) F2**
52	**9-983-718-01**	**KEY TOP (1) F3**
53	**9-983-719-01**	**KEY TOP (1) F4**
54	**9-983-720-01**	**KEY TOP (1) F5**
55	**9-983-721-01**	**KEY TOP (2) HOME**
56	**9-983-722-01**	**KEY TOP (2) STOP**
57	**9-983-723-01**	**KEY TOP (2) INS**
58	**9-983-724-01**	**KEY TOP (2) DEL**
59	**9-983-725-01**	**KEY TOP (2) RESET**
60	**9-984-250-01**	**KEY TOP (4) ESC**
61	**9-984-251-01**	**KEY TOP (5) TAB**
62	**9-984-252-01**	**KEY TOP (6) CTRL**
63	**9-984-253-01**	**KEY TOP (7) SHIFT**
64	**9-984-254-01**	**KEY TOP (8) CAP**
65	**9-985-314-01**	**KEY TOP (4) CODE**
66	**9-984-256-01**	**KEY TOP (5) BS**
67	**9-984-257-01**	**KEY TOP (9) RETURN**
68	**9-984-258-01**	**KEY TOP (10) SHIFT**
69	**9-984-255-01**	**KEY TOP (11) GRAPH**
70	**9-984-260-01**	**KEY TOP (11) SELECT**
71	**9-985-212-01**	**KEY TOP (3) 1**
72	**9-985-213-01**	**KEY TOP (3) 2**
73	**9-985-214-01**	**KEY TOP (3) 3**
74	**9-985-215-01**	**KEY TOP (3) 4**
75	**9-985-216-01**	**KEY TOP (3) 5**
76	**9-985-217-01**	**KEY TOP (3) 6**
77	**9-985-218-01**	**KEY TOP (3) 7**
78	**9-985-219-01**	**KEY TOP (3) 8**
79	**9-985-220-01**	**KEY TOP (3) 9**
80	**9-985-221-01**	**KEY TOP (3) 0**
81	**9-985-222-01**	**KEY TOP (3) —**
82	**9-985-223-01**	**KEY TOP (3) =**
83	**9-985-224-01**	**KEY TOP (3) **
84	**9-985-225-01**	**KEY TOP (3) Q**
85	**9-985-226-01**	**KEY TOP (3) W**
86	**9-985-227-01**	**KEY TOP (3) E**
87	**9-985-228-01**	**KEY TOP (3) R**
88	**9-985-229-01**	**KEY TOP (3) T**
89	**9-985-230-01**	**KEY TOP (3) Y**
90	**9-985-231-01**	**KEY TOP (3) U**
91	**9-985-232-01**	**KEY TOP (3) I**
92	**9-985-233-01**	**KEY TOP (3) O**
93	**9-985-234-01**	**KEY TOP (3) P**
94	**9-985-235-01**	**KEY TOP (3) [**
95	**9-985-236-01**	**KEY TOP (3)]**
96	**9-985-237-01**	**KEY TOP (3) A**
97	**9-985-238-01**	**KEY TOP (3) S**
98	**9-985-239-01**	**KEY TOP (3) D**
99	**9-985-240-01**	**KEY TOP (3) F**
100	**9-985-241-01**	**KEY TOP (3) G**
101	**9-985-242-01**	**KEY TOP (3) H**
102	**9-985-243-01**	**KEY TOP (3) J**
103	**9-985-244-01**	**KEY TOP (3) K**
104	**9-985-245-01**	**KEY TOP (3) L**
105	**9-985-246-01**	**KEY TOP (3) ;**
106	**9-985-247-01**	**KEY TOP (3) '**
107	**9-985-248-01**	**KEY TOP (3) £**
108	**9-985-249-01**	**KEY TOP (3) Z**
109	**9-985-250-01**	**KEY TOP (3) X**
110	**9-985-251-01**	**KEY TOP (3) C**
111	**9-985-252-01**	**KEY TOP (3) V**
112	**9-985-253-01**	**KEY TOP (3) B**
113	**9-985-254-01**	**KEY TOP (3) N**
114	**9-985-255-01**	**KEY TOP (3) M**
115	**9-985-256-01**	**KEY TOP (3) ,**
116	**9-985-257-01**	**KEY TOP (3) .**
117	**9-985-258-01**	**KEY TOP (3) /**
118	**9-985-259-01**	**KEY TOP (3)**
119	**9-985-260-01**	**KEY TOP (11) SPACE**
120	**9-984-310-01**	**KEY TOP (12) CURSOR**
121	9-984-312-01	CURSOR BAR (1)
122	9-984-313-01	CURSOR BAR (2)
123	9-985-261-01	SPACE BAR
124	**9-984-315-01**	**FRAME, KEYBOARD**
125	9-984-316-01	BAR HOLDER
126	**9-984-341-01**	**SPRING**
127	**4-605-117-01**	**SPRING**

NOTE:

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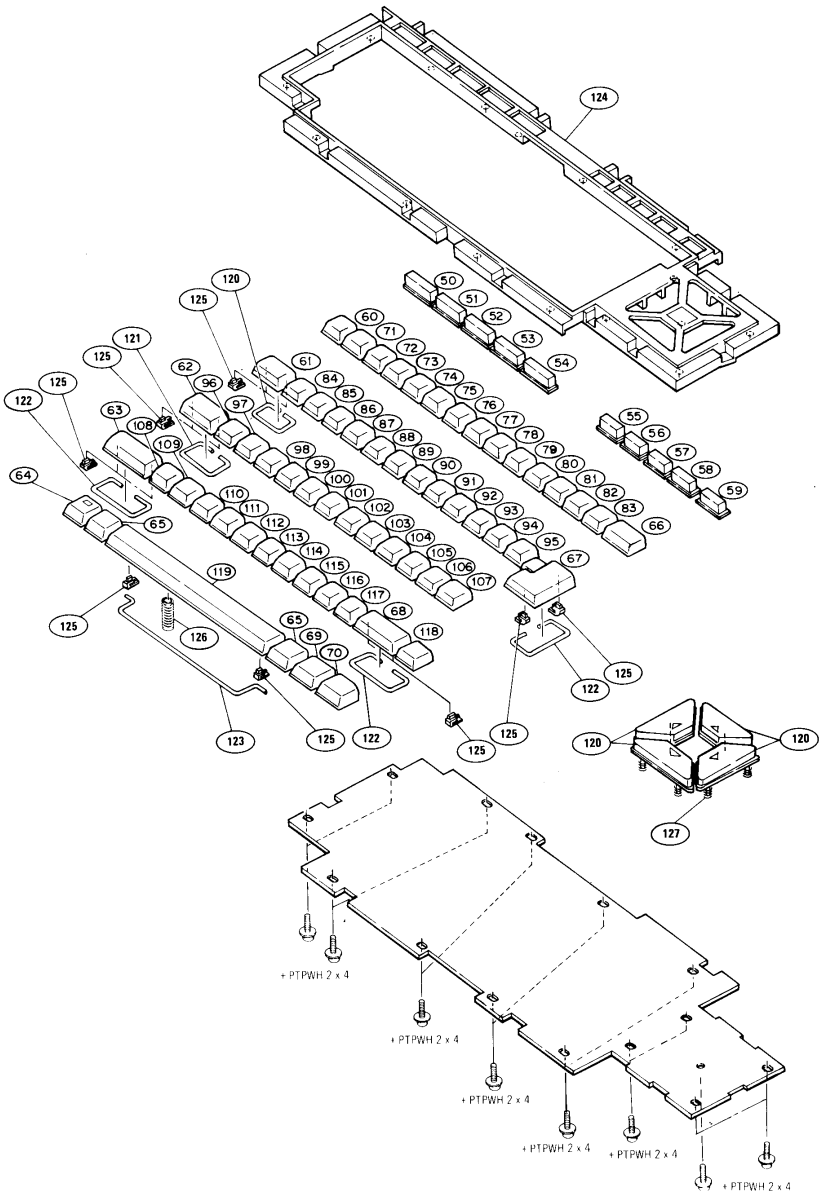
+ PTPWH 2 x 4
+ PTPWH 2 x 4
+ PTPWH 2 x 4
+ PTPWH 2 x 4
+ PTPWH 2 x 4
+ PTPWH 2 x 4

7-2. ELECTRICAL PARTS LIST

Ref. No.	Parts No.	Description
MAIN BOARD		
⚠	A-8050-098-A	MOUNTED CB, MAIN (75P/75B)
⚠	A-8050-100-A	MOUNTED CB, MAIN (55P)
	4-886-557-00	**CLIP (B), IC**
C1	**1-123-332-00**	**ELECT 47 20% 25V**
C2	**1-123-379-00**	**ELECT 0.47 20% 100V**
C3	**1-123-332-00**	**ELECT 47 20% 25V**
C4	**1-123-298-00**	**ELECT 470 20% 6.3V**
C5	**1-123-332-00**	**ELECT 47 20% 25V**
C6	**1-123-332-00**	**ELECT 47 20% 25V**
C7	**1-123-332-00**	**ELECT 47 20% 25V**
C8	**1-123-356-00**	**ELECT 10 20% 50V (75P/75B)**
C9	**1-123-356-00**	**ELECT 10 20% 50V (75P/75B)**
C10	**1-123-310-00**	**ELECT 470 20% 10V**
C11	**1-102-935-00**	**CERAMIC 2P 50V**
C12	**1-102-760-00**	**CERAMIC 68P 5% 50V**
C13	**1-102-508-00**	**CERAMIC 10P 50V**
C14	**1-123-356-00**	**ELECT 10 20% 50V (75P/75B)**
C15	**1-108-603-00**	**MYLAR 0.1 5% 50V**
C016	**1-102-760-00**	**CERAMIC 68P 5% 50V**
C017	**1-102-074-00**	**CERAMIC 0.001 5% 50V**
C018	**1-123-356-00**	**ELECT 10 20% 50V (75P/75B)**
C019	**1-123-356-00**	**ELECT 10 20% 50V**
C020	**1-108-603-00**	**MYLAR 0.1 5% 50V**
C021	**1-108-587-00**	**MYLAR 0.022 5% 50V**
C022	**1-123-379-00**	**ELECT 0.47 20% 100V**
C023	**1-102-905-00**	**CERAMIC 130P 5% 50V**
C024	**1-108-587-00**	**MYLAR 0.022 5% 50V**
C025	**1-108-587-00**	**MYLAR 0.022 5% 50V**
C026	**1-102-852-00**	**CERAMIC 47P 5% 50V**
C027	**1-123-307-00**	**ELECT 100 20% 10V**
C028	**1-102-936-00**	**CERAMIC 3P 50V**
C029	**1-130-640-00**	**FILM 0.47 5% 50V**
C030	**1-123-369-00**	**ELECT 4.7 20% 63V**
C031	**1-123-330-00**	**ELECT 22 20% 25V**
C032	**1-108-603-00**	**MYLAR 0.1 5% 50V**
C033	**1-102-514-00**	**CERAMIC 22P 5% 50V**
C034	**1-123-332-00**	**ELECT 47 20% 25V**
C035	**1-108-603-00**	**MYLAR 0.1 5% 50V**
C36	**1-108-603-00**	**MYLAR 0.1 5% 50V**
C37	**1-102-074-00**	**CERAMIC 0.001 5% 50V**
C38	**1-108-603-00**	**MYLAR 0.1 5% 50V**
C39	**1-108-587-00**	**MYLAR 0.022 5% 50V**
C40	**1-102-518-00**	**CERAMIC 33P 5% 50V**
C41	**1-123-369-00**	**ELECT 4.7 20% 63V**
C42	**1-123-369-00**	**ELECT 4.7 20% 63V**
C43	**1-102-074-00**	**CERAMIC 0.001 10% 50V**
C44	**1-123-332-00**	**ELECT 47 20% 25V**
C45	**1-123-369-00**	**ELECT 4.7 20% 63V**
C46	**1-102-518-00**	**CERAMIC 33P 5% 50V**
C47	**1-102-518-00**	**CERAMIC 33P 5% 50V**
C48	**1-102-514-00**	**CERAMIC 22P 5% 50V**
C49	**1-123-332-00**	**ELECT 47 20% 25V**
C50		
C51	**1-108-587-00**	**MYLAR 0.022 5% 50V**
C52	**1-123-369-00**	**ELECT 4.7 20% 63V**
C53	**1-108-587-00**	**MYLAR 0.022 5% 50V**
C54	**1-123-332-00**	**ELECT 47 20% 25V**
C55	**1-123-332-00**	**ELECT 47 20% 25V**
C56	**1-108-579-00**	**MYLAR 0.01 5% 50V**
C57	**1-123-308-00**	**ELECT 220 20% 10V**
C58	**1-108-587-00**	**MYLAR 0.022 5% 50V**
C59	**1-123-332-00**	**ELECT 47 20% 25V**
C60	**1-123-332-00**	**ELECT 47 20% 25V**
C61	**1-123-369-00**	**ELECT 4.7 20% 63V**
C62	**1-123-369-00**	**ELECT 4.7 20% 63V**
C63	**1-123-369-00**	**ELECT 4.7 20% 63V**
C64	**1-123-369-00**	**ELECT 4.7 20% 63V**
C66	**1-123-332-00**	**ELECT 47 20% 25V (55P)**
C67	**1-123-332-00**	**ELECT 47 20% 25V (55P)**
C68	**1-123-332-00**	**ELECT 47 20% 25V**
C69	**1-161-974-00**	**CERAMIC 0.1 16V**
C70	**1-161-974-00**	**CERAMIC 0.1 16V**
C73	**1-123-298-00**	**ELECT 470 20% 6.3V**
C79	**1-102-514-00**	**CERAMIC 22P 5% 50V**
C101	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C102	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C103	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C104	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C105	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C106	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C107	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C108	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C109	**1-162-113-00**	**CERAMIC 0.01 30% 16V**

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Ref. No.	Parts No.	Description
C110	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C111	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C112	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C113	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C114	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C115	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C116	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C117	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C118	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C119	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C120	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C121	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C122	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C123	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C124	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C125	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C126	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C127	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C128	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C129	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C130	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C131	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C132	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C133	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C134	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C135	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C136	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C137	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C138	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C139	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C140	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C141	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C142	**1-162-113-00**	**CERAMIC 0.01 30% 16V (55P)**
C143	**1-162-113-00**	**CERAMIC 0.01 30% 16V (55P)**
C144	**1-162-113-00**	**CERAMIC 0.01 30% 16V (55P)**
C145	**1-162-113-00**	**CERAMIC 0.01 30% 16V (55P)**
C146	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C147	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C148	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C149	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C150	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C151	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C152	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C153	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C154	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C155	**1-162-113-00**	**CERAMIC 0.01 30% 16V**
C156	**1-162-113-00**	**CERAMIC 0.01 30% 16V**

Ref. No.	Parts No.	Description
CN1	**1-562-383-00**	**50P**
CN2	**1-562-626-11**	**50P**
CN3	**1-561-534-00**	**21P (75P/75B)**
CN4	**1-564-373-11**	**14P**
CN5	**1-561-468-00**	**8P**
CN8	**1-564-372-00**	**9P**
CN9	**1-564-372-00**	**9P**
CN10	1-564-674-11	8P
CN11	1-564-376-11	13P
CN12	1-564-377-11	9P
D1	**8-719-101-49**	**RD5.1EL1**
D2	**8-719-901-59**	**KV1320**
D3	**8-719-815-55**	**1S1555**
D4	**8-719-815-55**	**1S1555**
D5	**8-719-815-55**	**1S1555**
D6	**8-719-200-02**	**10E-2**
D7	**8-719-815-55**	**1S1555**
DL1	**1-415-374-11**	**DELAY LINE (Y-DL)**
IC1	**8-759-900-04**	**SN74LS04N**
IC2	**8-759-908-94**	**TMS9929ANL**
IC3	**8-759-101-91**	**UPD416C-2**
IC4	**8-759-101-91**	**UPD416C-2**
IC5	**8-759-101-91**	**UPD416C-2**
IC6	**8-759-101-91**	**UPD416C-2**
IC7	**8-757-925-00**	**CX-7925A**
IC8	**8-759-900-74**	**SN74LS74AN**
IC9	**8-759-101-91**	**UPD416C-2**
IC10	**8-759-101-91**	**UPD416C-2**
IC11	**8-759-101-91**	**UPD416C-2**
IC12	**8-759-101-91**	**UPD416C-2**
IC13	**8-759-938-89**	**LM1889N**
IC14	**8-759-140-66**	**UPD4066BC**
IC15	**8-759-900-74**	**SN74LS74AN**
IC16	**8-759-182-55**	**UPD8255AC-5**
IC17	**8-759-901-53**	**SN74LS153N**
IC18	**8-759-901-39**	**SN74LS139N**
IC19	**8-759-131-11**	**UPC311C**
IC21	**8-759-900-74**	**SN74LS74AN**

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Ref. No.	Parts No.	Description
IC22	8-759-901-45	SN74LS145N
IC23	8-759-901-39	SN74LS139N
IC24	8-759-900-32	SN74LS32N
IC25	8-759-900-86	SN74LS86N
IC26	8-759-900-04	SN74LS04N
IC27	8-759-900-00	SN74LS00N
IC28	8-759-900-02	SN74LS02N
IC29	8-759-900-04	SN74LS04N
IC30	8-759-900-27	SN74LS27N
IC31	8-759-901-75	SN74LS175N
IC32	8-759-900-08	SN74LS08N
IC33	8-759-901-26	SN74LS126AN
IC34	8-759-900-74	SN74LS74AN
IC35	8-759-900-74	SN74LS74AN
IC36	8-759-900-11	SN74LS11N
IC37	8-759-900-08	SN74LS08N
IC38	8-759-900-04	SN74LS04N
IC39	8-759-903-73	SN74LS373N
IC40	8-759-906-45	SN74LS645N
IC41	8-759-916-80	LH0080A
IC42	8-759-915-71	MSM38256-70RS
IC43		
IC44	8-759-915-23	MSM38128A-77RS
IC45	8-759-900-10	SN74LS10N
IC46	8-759-900-32	SN74LS32N
IC47	8-759-903-67	SN74LS367N
IC48	8-759-908-60	AY-3-8910
IC49	8-759-901-57	SN74LS157N
IC50	8-759-900-74	SN74LS74AN
IC51	8-759-900-74	SN74LS74AN
IC52	8-759-900-02	SN74LS02N
IC53	8-759-900-27	SN74LS27N
IC54	8-759-903-67	SN74LS367N
IC55	8-759-903-67	SN74LS367N
IC56	8-759-903-67	SN74LS367N
IC57	8-759-901-57	SN74LS157N
IC58	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)
IC59	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)
IC60	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)
IC61	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)

Ref. No.	Parts No.	Description
IC62	8-759-901-57	SN74LS157N
IC63	8-759-901-57	SN74LS157N
IC64	8-759-900-09	SN74LS09N
IC65	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)
IC66	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)
IC67	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)
IC68	8-759-905-75	MSM3764-15RS (75P/75B)
	8-759-101-91	UPD416C-2 (55P)
L1	1-408-413-00	22
L2	1-410-222-11	8.2
L3	1-408-411-00	15
L4	1-408-416-00	39
L5	1-408-420-00	82
L6	1-408-420-00	82
Q1	8-729-612-77	2SA1027R (75P/75B)
Q2	8-729-663-47	2SC1364 (75P/75B)
Q3	8-729-612-77	2SA1027R (75P/75B)
Q4	8-729-663-47	2SC1364 (75P/75B)
Q5	8-729-612-77	2SA1027R (75P/75B)
Q6	8-729-663-47	2SC1364 (75P/75B)
Q7	8-729-663-47	2SC1364 (75P/75B)
Q8	8-729-100-13	2SC2001
Q9	8-729-663-47	2SC1364
Q10	8-729-663-47	2SC1364
Q11	8-729-612-77	2SA1027R
Q12	8-729-663-47	2SC1364
Q13	8-729-663-47	2SC1364
Q14	8-729-663-47	2SC1364 (75P/75B)
Q15	8-729-663-47	2SC1364
Q16	8-729-663-47	2SC1364
Q17	8-729-612-77	2SA1027R
Q18	8-729-663-47	2SC1364
Q19	8-729-663-47	2SC1364
Q20	8-729-663-47	2SC1364
Q21	8-729-203-04	2SK30A
Q22	8-729-663-47	2SC1364
Q23	8-729-364-12	2SC641K
Q24	8-729-364-12	2SC641K
Q25	8-729-663-47	2SC1364

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Ref. No.	Parts No.	Description
R61	1-247-815-00	CARBON 220 5% 1/6W
R62	1-247-851-00	CARBON 6.8K 5% 1/6W
R63	1-247-847-00	CARBON 4.7K 5% 1/6W
R64	1-247-837-00	CARBON 1.8K 5% 1/6W
R65	1-247-849-00	CARBON 5.6K 5% 1/6W
R66	1-247-849-00	CARBON 5.6K 5% 1/6W
R67	1-247-855-00	CARBON 10K 5% 1/6W
R68	1-247-849-00	CARBON 5.6K 5% 1/6W
⚠R69	1-247-239-00	CARBON 910 5% 1/2W
R70	1-247-863-00	CARBON 22K 5% 1/6W
R71	1-247-863-00	CARBON 22K 5% 1/6W
R72	1-247-863-00	CARBON 22K 5% 1/6W
R73	1-247-815-00	CARBON 220 5% 1/6W
R74	1-247-871-00	CARBON 47K 5% 1/6W
R75	1-247-831-00	CARBON 1K 5% 1/6W
R76	1-247-831-00	CARBON 1K 5% 1/6W
R77	1-247-879-00	CARBON 100K 5% 1/6W
R78	1-247-879-00	CARBON 100K 5% 1/6W
R79	1-247-843-00	CARBON 3.3K 5% 1/6W
R80	1-247-783-00	CARBON 10 5% 1/6W
R81	1-247-821-00	CARBON 390 5% 1/6W
R82	1-247-859-00	CARBON 15K 5% 1/6W
R83	1-247-839-00	CARBON 2.2K 5% 1/6W
R84	1-247-841-00	CARBON 2.7K 5% 1/6W
R85	1-247-831-00	CARBON 1K 5% 1/6W
R86	1-247-833-00	CARBON 1.2K 5% 1/6W
R87	1-247-843-00	CARBON 3.3K 5% 1/6W
R88	1-247-849-00	CARBON 5.6K 5% 1/6W
R89	1-247-819-00	CARBON 330 5% 1/6W
R90	1-247-795-00	CARBON 33 5% 1/6W
R91	1-247-831-00	CARBON 1K 5% 1/6W
R92	1-247-817-00	CARBON 270 5% 1/6W
R93	1-247-821-00	CARBON 390 5% 1/6W
R94	1-247-831-00	CARBON 1K 5% 1/6W
R95	1-247-819-00	CARBON 330 5% 1/6W
R96	1-247-849-00	CARBON 5.6K 5% 1/6W
R97	1-247-847-00	CARBON 4.7K 5% 1/6W
R98	1-247-831-00	CARBON 1K 5% 1/6W
R99	1-247-823-00	CARBON 470 5% 1/6W
R100	1-247-837-00	CARBON 1.8K 5% 1/6W
R101	1-247-837-00	CARBON 1.8K 5% 1/6W
R102	1-247-841-00	CARBON 2.7K 5% 1/6W
R103	1-247-835-00	CARBON 1.5K 5% 1/6W
R104	1-247-855-00	CARBON 10K 5% 1/6W
R105	1-247-831-00	CARBON 1K 5% 1/6W

Ref. No.	Parts No.	Description
R106	1-247-855-00	CARBON 10K 5% 1/6W
R107	1-247-831-00	CARBON 1K 5% 1/6W
R108	1-247-841-00	CARBON 2.7K 5% 1/6W
R109	1-247-799-00	CARBON 47 5% 1/6W
R110	1-247-855-00	CARBON 10K 5% 1/6W
R111	1-247-819-00	CARBON 330 5% 1/6W
R112	1-247-879-00	CARBON 100K 5% 1/6W
R113	1-247-871-00	CARBON 47K 5% 1/6W
R114	1-247-863-00	CARBON 22K 5% 1/6W
R115	1-247-855-00	CARBON 10K 5% 1/6W
R116	1-247-831-00	CARBON 1K 5% 1/6W
R117	1-247-863-00	CARBON 22K 5% 1/6W
R118	1-247-871-00	CARBON 47K 5% 1/6W
R119	1-247-831-00	CARBON 1K 5% 1/6W
R120	1-247-841-00	CARBON 2.7K 5% 1/6W
R121	1-247-841-00	CARBON 2.7K 5% 1/6W
R122	1-247-791-00	CARBON 22 5% 1/6W
R123	1-247-841-00	CARBON 2.7K 5% 1/6W
R124	1-247-841-00	CARBON 2.7K 5% 1/6W
R125	1-247-841-00	CARBON 2.7K 5% 1/6W
R126	1-247-791-00	CARBON 22 5% 1/6W
R127	1-247-791-00	CARBON 22 5% 1/6W
R128	1-247-791-00	CARBON 22 5% 1/6W
R129	1-247-841-00	CARBON 2.7K 5% 1/6W
R130	1-247-855-00	CARBON 10K 5% 1/6W
R131	1-247-839-00	CARBON 2.2K 5% 1/6W
R132	1-247-821-00	CARBON 390 5% 1/6W
R133	1-247-841-00	CARBON 2.7K 5% 1/6W
R134	1-247-841-00	CARBON 2.7K 5% 1/6W
R135	1-247-887-00	CARBON 220K 5% 1/6W
R136	1-247-863-00	CARBON 22K 5% 1/6W
RY1	1-515-520-00	RELAY
VC1	1-141-227-00	TRIMAR, CERAMIC 20P
VC2	1-141-227-00	TRIMAR, CERAMIC 20P
VR1	1-226-710-00	ADJ, SOLID 10K(75P/75B)
VR2	1-226-710-00	ADJ, SOLID 10K(75P/75B)
VR3	1-226-710-00	ADJ, SOLID 10K(75P/75B)
VR4	1-226-707-00	ADJ, SOLID 1K
X1	1-567-161-00	CRYSTAL, 10.73868MHz

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FUSE, LED, POWER, 5V, 12V

Ref. No.	Parts No.	Description
FUSE BOARD		
	1-533-162-00	**HOLDER, FUSE**
	1-613-627-11	PC BOARD, FUSE
⚠**C9**	**1-161-953-00**	**CERAMIC 0.0047 20% 400V**
F401	**1-532-612-00**	**TIME-LAG 160mA**
LED BOARD		
D1	**8-719-908-47**	**SLP171D**
POWER BOARD		
	A-8050-103-A	MOUNTED CB, POWER (75B) (WITH +5V, 12V BOARD)
	A-8050-102-A	MOUNTED CB, POWER (55P/75P) (WITH +5V, 12V BOARD)
	1-464-383-11	**MODULATOR, RF (75B)**
	1-464-384-11	**MODULATOR, RF (55P/75P)**
C1	**1-125-375-11**	**ELECT(BLOCK) 10000 20% 16V**
C2	**1-125-376-11**	**ELECT(BLOCK) 3300 20% 25V**
C3	**1-123-362-00**	**ELECT 330 20% 50V**
C4	**1-123-332-00**	**ELECT 47 20% 25V**
C5	**1-136-171-00**	**FILM 0.33 5% 50V**
C8	**1-123-332-00**	**ELECT 47 20% 25V**
CN1	**1-562-121-00**	**6P**
CN2	**1-560-200-00**	**2P**
CN3	**1-562-327-00**	**3P**
CN4	**1-562-327-00**	**3P**
CN5	**1-564-675-11**	**8P**
CN6	**1-562-250-00**	**5P**

Ref. No.	Parts No.	Description
D1	**8-719-200-02**	**10E2**
D2	**8-719-200-02**	**10E2**
D3	**8-719-200-02**	**10E2**
D4	**8-719-200-02**	**10E2**
D6	**8-719-300-57**	**RB402**
IC3	**8-759-700-69**	**NJM79L12A**
L1	**1-408-413-00**	**MICRO INDUCTOR 22**
L2	**1-543-184-00**	**BEAD, FERRITE**
R1	**1-247-837-00**	**CARBON 1.8K 5% 1/6W**
R2	**1-247-837-00**	**CARBON 1.8K 5% 1/6W**
R3	**1-247-831-00**	**CARBON 1K 5% 1/6W**
5V BOARD		
	1-613-624-11	PC BOARD, +5V
C6	**1-123-332-00**	**ELECT 47 20% 25V**
C10	**1-136-171-00**	**FILM 0.33 5% 50V**
IC1	**8-749-930-52**	**SI-3052V**
12V BOARD		
	1-613-625-11	PC BOARD, +12V
C7	**1-123-332-00**	**ELECT 47 20% 25V**
C11	**1-136-171-00**	**FILM 0.33 5% 50V**
IC2	**8-749-931-22**	**SI-3122V**

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KEYBOARD (HB-55P)

Ref. No.	Parts No.	Description
	1-464-382-11	KEYBOARD UNIT (HB-55P)
D1~D3	**8-719-815-55**	**1S1555**
D4	**9-983-904-01**	**LN01201C**
S1~S9	**9-983-791-01**	**KEY BOARD**
S10	**9-984-704-01**	**KEY BOARD (RESET)**
S11~S53	**9-983-791-01**	**KEY BOARD**
S54	**9-984-704-01**	**KEY BOARD (SHIFT)**
S55~S65	**9-983-791-01**	**KEY BOARD**
S66	**9-984-704-01**	**KEY BOARD (SHIFT)**
S67	**9-983-791-01**	**KEY BOARD**
S68, S69	**9-984-704-01**	**KEY BOARD (SPACE, CODE)**
S70~S74	**9-983-791-01**	**KEY BOARD**

FRAME (HB-55P/75P/75B)

Ref. No.	Parts No.	Description
⚠CN401	**1-534-817-XX**	**CORD, POWER, FULO PLUG (55P/75P)**
	1-551-884-00	**CORD, POWER (75B)**
⚠S401	**1-553-318-00**	**POWER**
⚠T401	**1-447-939-11**	**POWER**

KEYBOARD (HB-75P/75B)

	1-464-381-11	KEYBOARD UNIT (HB-75P/75B)
D1~D3	**8-719-815-55**	**1S1555**
S1~S10	**1-552-539-11**	**KEY BOARD (1)**
S11~S65	**9-985-263-01**	**KEY BOARD (2)**
S66	**9-984-340-01**	**KEY BOARD (3) WITH LED**
S67~S71	**9-985-263-01**	**KEY BOARD (2)**
S72~S75	**1-552-539-11**	**KEY BOARD (1)**

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MAIN

Ref. No.	Parts No.	Description
Q26	8-729-663-47	2SC1364
Q27	8-729-663-47	2SC1364
Q28	8-729-203-04	2SK30A
R1	1-247-807-00	CARBON 100 5% 1/6W (75P/75B)
R2	1-247-815-00	CARBON 220 5% 1/6W (75P/75B)
R3	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R4	1-247-895-00	CARBON 470K 5% 1/6W (75P/75B)
R5	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R6	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R7	1-247-879-00	CARBON 100K 5% 1/6W (75P/75B)
R8	1-247-855-00	CARBON 10K 5% 1/6W
R9	1-247-803-00	CARBON 68 5% 1/6W
R10	1-247-811-00	CARBON 150 5% 1/6W
R11	1-247-831-00	CARBON 1K 5% 1/6W
R12	1-247-843-00	CARBON 3.3K 5% 1/6W
R13	1-247-831-00	CARBON 1K 5% 1/6W
R14	1-247-815-00	CARBON 220 5% 1/6W
R15	1-247-807-00	CARBON 100 5% 1/6W (75P/75B)
R16	1-247-815-00	CARBON 220 5% 1/6W (75P/75B)
R17	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R18	1-247-895-00	CARBON 470K 5% 1/6W (75P/75B)
R19	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R20	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R21	1-247-879-00	CARBON 100K 5% 1/6W (75P/75B)
R22	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R23	1-247-817-00	CARBON 270 5% 1/6W
R24	1-247-807-00	CARBON 100 5% 1/6W (75P/75B)
R25	1-247-815-00	CARBON 220 5% 1/6W (75P/75B)
R26	1-247-843-00	CARBON 3.3K 5% 1/6W (75P/75B)
R27	1-247-895-00	CARBON 470K 5% 1/6W (75P/75B)
R28	1-247-859-00	CARBON 15K 5% 1/6W (75P/75B)
R29	1-247-861-00	CARBON 18K 5% 1/6W (75P/75B)
R30	1-247-879-00	CARBON 100K 5% 1/6W (75P/75B)
R31	1-247-831-00	CARBON 1K 5% 1/6W
R32	1-247-823-00	CARBON 470 5% 1/6W
R33	1-247-831-00	CARBON 1K 5% 1/6W
R34	1-247-823-00	CARBON 470 5% 1/6W
R35	1-247-859-00	CARBON 15K 5% 1/6W
R36	1-247-867-00	CARBON 33K 5% 1/6W
R37	1-247-887-00	CARBON 220K 5% 1/6W
R38	1-247-847-00	CARBON 4.7K 5% 1/6W
R39	1-247-843-00	CARBON 3.3K 5% 1/6W
R40	1-247-855-00	CARBON 10K 5% 1/6W
R41	1-247-847-00	CARBON 4.7K 5% 1/6W
R42	1-247-835-00	CARBON 1.5K 5% 1/6W
R43	1-247-825-00	CARBON 560 5% 1/6W
R44	1-247-847-00	CARBON 4.7K 5% 1/6W (75P/75B)
R45	1-247-855-00	CARBON 10K 5% 1/6W (75P/75B)
R46	1-247-851-00	CARBON 6.8K 5% 1/6W (75P/75B)
R47	1-247-851-00	CARBON 6.8K 5% 1/6W (75P/75B)
R48	1-247-855-00	CARBON 10K 5% 1/6W (75P/75B)
R49	1-247-851-00	CARBON 6.8K 5% 1/6W
R50	1-247-855-00	CARBON 10K 5% 1/6W
R51	1-247-847-00	CARBON 4.7K 5% 1/6W (75P/75B)
R52	1-247-831-00	CARBON 1K 5% 1/6W (75P/75B)
R53	1-247-831-00	CARBON 1K 5% 1/6W (75P/75B)
R54	1-247-831-00	CARBON 1K 5% 1/6W
R55	1-247-823-00	CARBON 470 5% 1/6W
R56	1-247-819-00	CARBON 330 5% 1/6W
R57	1-247-889-00	CARBON 270K 5% 1/6W
R58	1-247-831-00	CARBON 1K 5% 1/6W
R59	1-247-839-00	CARBON 2.2K 5% 1/6W
R60	1-247-811-00	CARBON 150 5% 1/6W

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1. **The shaded and ⚠-marked components are critical to safety.**
   Replace only with same components as specified.

2. Parts printed in **Bold-Face type** are normally stocked for replacement purposes. The remaining parts shown in this manual are not normally required for routine service work. Orders for parts not shown in Bold-Face type will be processed, but allow for additional delivery time.