SVI-738 X'PRESS
COMPUTER SYSTEM

SERVICE & TECHNICAL MANUAL

EDITED BY

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SVI
SPECTRAVIDEO

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Kimba Lau

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INTRODUCTION

Scope

This manual is designed to assist the experienced and inexperienced service technician in locating and repairing problems that may occur in SVI-728 computer and its peripherals. This manual will cover all necessary information and clues for technical reference and servicing use. A spare part listing could be found in appendix for spare part order via our local agent.

There are 6 chapters, 3 appendices in this manual. Chapter 1 explains the basic configuration and the system architecture of SVI-738 X'PRESS.

Chapter 2 and 3 gives the details I/O specification and memory mapping of the individual ports.

Chapter 4 is a quick run down of the peripherals support and its specification for the X'PRESS.

Chapter 5 and 6 is the heart of servicing part. It consists of detail assembly and disassembly procedures, diagnostic routine, cautions, recover routine, ..., etc.

The appendices includes detail spare part list, circuit diagram, software listing for reference and development needs.

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CHAPTER 1

SYSTEM CONFIGURATIONS AND ARCHITECTURE

1.1 WHAT IS X'PRESS?

Following the success of the MSX home computer standard, Spectravideo International Limited continues to strengthen their leading position in MSX series computer. Well before any new challenge occurred, Spectravideo has already had the X'PRESS ready in August 1985 with the most outstanding features to beat the competitors. The features include an attractive ergonomically-designed console with multi-function retractable handle, and there is more to be seen electronically. First, a standard 3 1/2" microfloppy drive together with the RS-232C interface makes the X'PRESS not just a computer for games. Secondly, the new VDP (V9938) means that the X'PRESS can offer software switching between 40 and 80 column. Thirdly, in order to bridge the gap of lacking support in business and personal application software in MSX. X'PRESS includes the CP/M compatibility to make it a all round machine (see appendix D for software support in 3 1/2" format). The system architecture can be seen in Section 1.3.

1.2 BASIC SPECIFICATION

A. LSI

- CPU — Z80A
  Clock 3.58MHz (colour Subcarrier Frequency)
  1 Wait Cycle in M1
- VDP — V9938
  2 x 4416 (16K)
  Clock 21.477 MHz
- PSG — AY-3-8910
- PPI — 2 x customized ULA
- FDC — 1793
- RS-232C — 8251 and 8253
  Clock 1.8432 Hz
- DRIVE — Built-in 3 1/2" Microfloppy + an optional drive

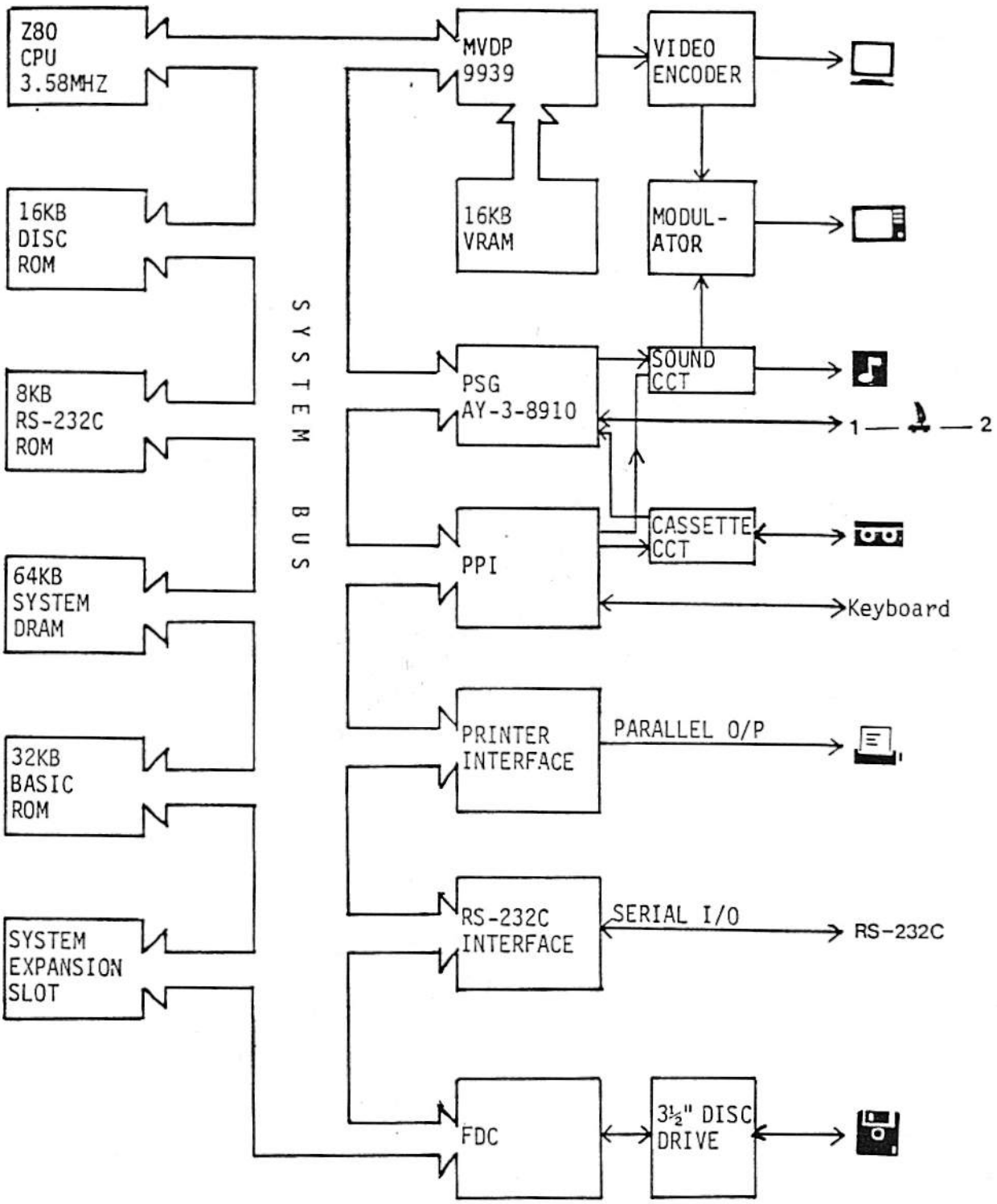
B. MEMORY

- ROM — This 32KB ROM contains the MSX BASIC interpreter programme as well as the monitor programme.
  16KB Disk I/O Driver programme in slot 3-1 and 8KB RS232 monitor programme in slot 3-0.

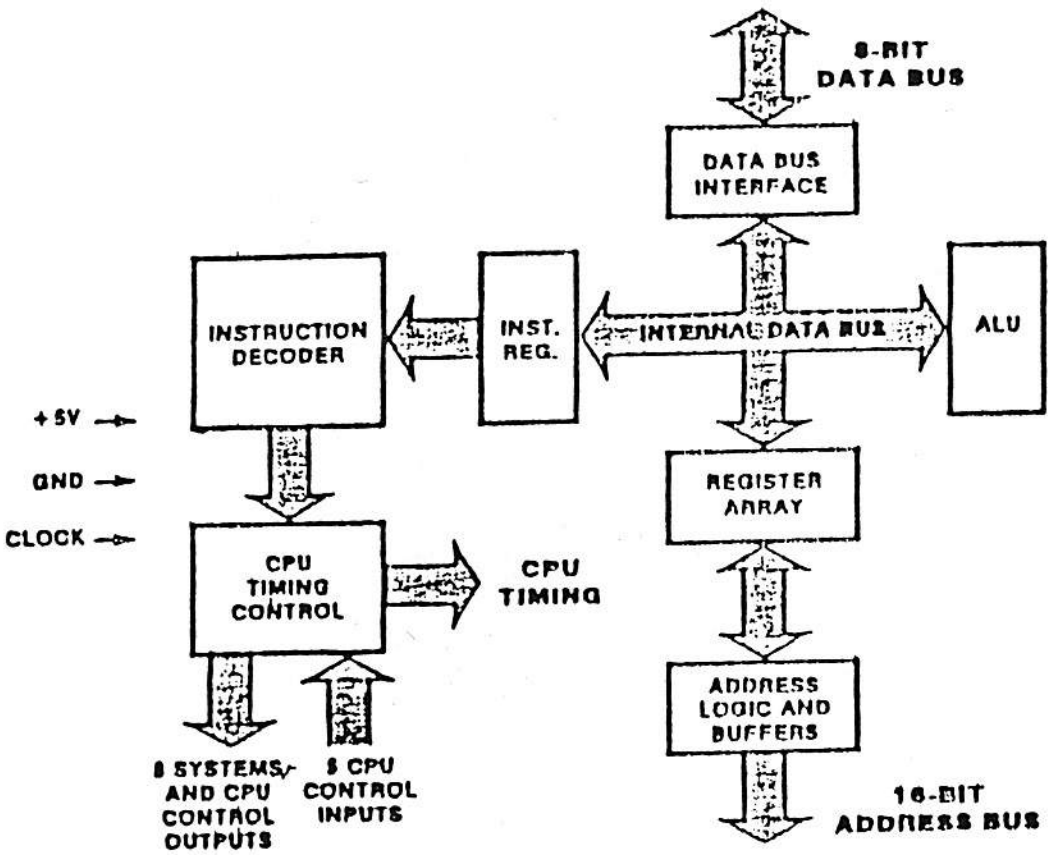
- RAM — 64K Bytes

- Basic ROM starts from 0000H to 7FFFH; and RAM starts from FFFFH and grows downward on the memory map. (Refer to Chapter 3 - memory map for the details)

1.3 SVI-738 SYSTEM ARCHITECTURE



1.4 Z80A MICROPROCESSOR



Z80 CPU Block Diagram

Detail information about Z80 CPU, please refer to books or catalogues published by I.C. manufacturer.

1.5 MSX VIDEO DISPLAY PROCESSOR

X'PRESS is the first MSX machine to use V9938 Video Display Processor which will be a standard VDP for MSX2. Here is a brief description of the text mode used in X'PRESS. Please refer to MSX-VDP (Yamaha V9938) user's manual for detail operation.

REGISTER TYPES

The MSX-VIDEO DATA PROCESSOR (MSX-VDP) has four eight-bit ports (PORT 0 to PORT 3) for exchanging data from a Central Processing Unit (CPU), the MSX-VDP registers, and the computer's Video RAM (VRAM).

All registers of the MSX-VDP are eight bits wide and can be divided into the following three types.

1. Control Registers

   Registers R0 to R23 and R32 to R46 (total 39) are primarily write registers.

2. Pallete Registers

   Registers P0 to P15 (total 16) are primarily write registers.

3. Status Registers

   Registers S0 to S9 (total 10) are primarily output registers.

CPU

PORT 0 (R/W)	PORT 1 (R/W)	PORT 2 (W)	PORT 3 (W)
Control Register (W) #0 to #23	Status Register (R) #0 to #9	Palette Register (W) #0 to #15	Video RAM 128K bytes (R/W)
Control Register (W) #32 to #46	MSX-VDP		Expanded RAM 64K bytes (R/W)

1. Accessing the Control Registers

There are two ways to set data in the MSX-VDP control registers (R#0 to R#46), which we will outline below.

1.1 Direct Access

Output the data and the register number in order. Since this order is always used, be careful during access to MSX-VDP for an interrupt routine.

	MSB	7	6	5	4	3	2	1	0	LSB
Port #1	First byte	D7	D6	D5	D4	D3	D2	D1	D0	DATA
	Second byte	1	0	R5	R4	R3	R2	R1	R0	REGISTER #

1.2 Indirect Access

Specify the register number in control register R#17 (Control Register Pointer).

First set the register number in R#17 (using direct specification) by outputting data to Port #3. When you set the data in R#17, you can also set its MSB to control autoincrementing.

If autoincrementing is prohibited, the contents of R#17 are not changed, and thus you do not have to reset R#17.

	MSB	7	6	5	4	3	2	1	0	LSB
Register #17		AII	0	R5	R4	R3	R2	R1	R0	REGISTER #

AII
- 1: Auto increment inhibit
- 0: Auto increment on

Port #3	First byte	D7	D6	D5	D4	D3	D2	D1	D0	DATA
Port #3	Second byte	D7	D6	D5	D4	D3	D2	D1	D0	DATA
Port #3	nth byte	D7	D6	D5	D4	D3	D2	D1	D0	DATA

2. Accessing the Pallete Registers

To set data in the MSX-VDP palette registers (P#0 to P#15/9 bit), you must first set the palette register number in register R#16 (Color palette address pointer) then output the two bytes of data in order through port #2.

	MSB	7	6	5	4	3	2	1	0	LSB
		0	0	0	0	C3	C2	C1	C0	Pallete #
Port #2 First byte		0	R2	R1	R0	0	B2	B1	B0	DATA
			Red data				Blue data			
Port #2 Second byte		0	0	0	0	0	G2	G1	G0	DATA
							Green data			

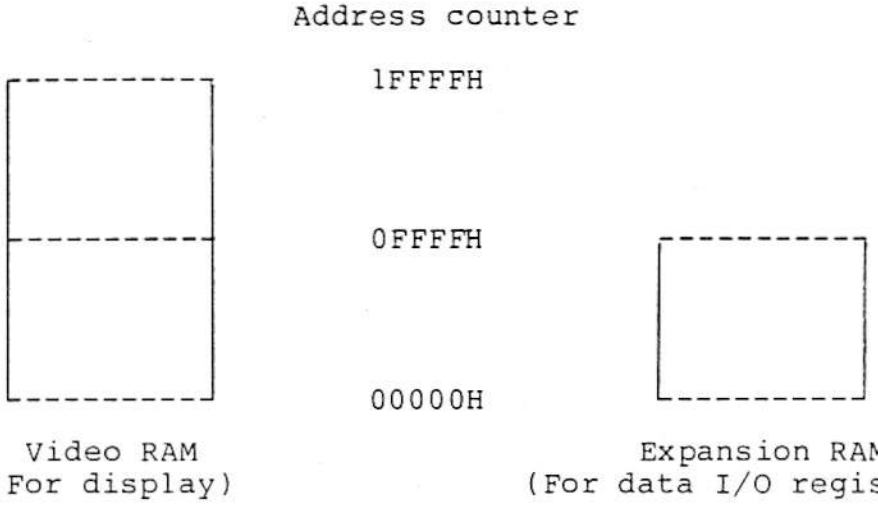
3. Accessing the Status Registers

To read the status registers of MSX-VDP (S#0 to S#9), you must first set the register number in R#15 (Status register pointer) and read the data through Port #1.

	MSB	7	6	5	4	3	2	1	0	LSB
		0	0	0	0	C3	C2	C1	C0	Status register #
Port #1 Read data		D7	D6	D5	D4	D3	D2	D1	D0	DATA

4. Accessing the Video RAM

A Video RAM of 128K bytes plus an expansion RAM of 64K bytes can be connected to MSX-VDP. The memory maps for these areas are shown in the map below.



Accessing memory

To access memory, the following order must be followed.

1. Switch banks (VRAM to Expansion RAM)
2. Set the address counter (A16 to A14)
3. Set the address counter (A7 to A0)
4. Set the address counter (A13 to A8) and specify read or write
5. Read or write the data

1. Switching Banks (VRAM to Expansion RAM)

Since the contents of R#45 (Argument register) do not change each time that memory is accessed, it is not necessary to respecify bit 6 or R#45, which specifies banking, every time banking is to be done.

	MSB 7	6	5	4	3	2	1	0 LSB
Register #45	0	MXC	MXD	MXS	KIY	DIX	EQ	MAJ Argument register

--- 1: Expansion RAM
--- 0: Video RAM

2. Setting the Address Counter (A16-A14)

Set the high-order three bits (A16 to A14) of the address counter using register R#14 (VRAM Access base address register).

	MSB 7	6	5	4	3	2	1	0 LSB
Register #14	0	0	0	0	0	A16	A15	A14 VRAM Access base register

3. Setting the Address Counter (A7 to A0)

Set the low-order eight bits (A7 to A0) of the address counter by outputting data to Port #1.

	MSB 7	6	5	4	3	2	1	0	LSB
Port #1	A7	A6	A5	A4	A3	A2	A1	A0	First byte

4. Setting the Address Counter (A13 to A8) and Specifying Read or Write

Set the remaining six bits (A13 to A8) of the address counter and specify read or write by outputting data to Port #1.

	MSB 7	6	5	4	3	2	1	0	LSB
Port #1	X	X	A13	A12	A11	A10	A9	A8	Second byte
	|	|						
	0	0: Read							
	0	1: Write							

5. Reading or Writing Data

Since the address counter is automatically incremented when data is read from or written to Port #0, you can continually access blocks of data.

* To access the VRAM, you can also use commands. These commands will be explained in a later chapter.

* Refer to the data sheet for access timings.

TEXT 1 MODE

Characteristics

- Pattern size	6 dots (w) x 8 dots (h)
- Patterns	256 types
- Screen pattern count	40 (w) x 24 (h) patterns
- Pattern colors	Two colors out of 512 colors (per screen)
- VRAM area per screen	4K bytes

Controls

- Pattern font	VRAM pattern generator table
- Screen pattern location	VRAM pattern name table
- Pattern color code 1	High-order four bits of R#7
- pattern color code 0	Low-order four bits of R#7
- Background color code	Low-order four bits of R#7

1. Mode and Register Settings

	MSB 7	6	5	4	3	2	1	0 LSB	
R#0	0	DG	IE2	IE1	0*	0*	0*	0	Mode register 0
R#1	0	BL	IE0	1*	0*	0	SI	MAG	Mode register 1
R#8	MS	LP	TP	CB	VR	0	SP	BW	Mode register 2
R#9	0	0	S1	S0	IL	EO	NT	DC	Mode register 3

* Examples of settings in TEXT 1 mode
All other bits are set accordingly

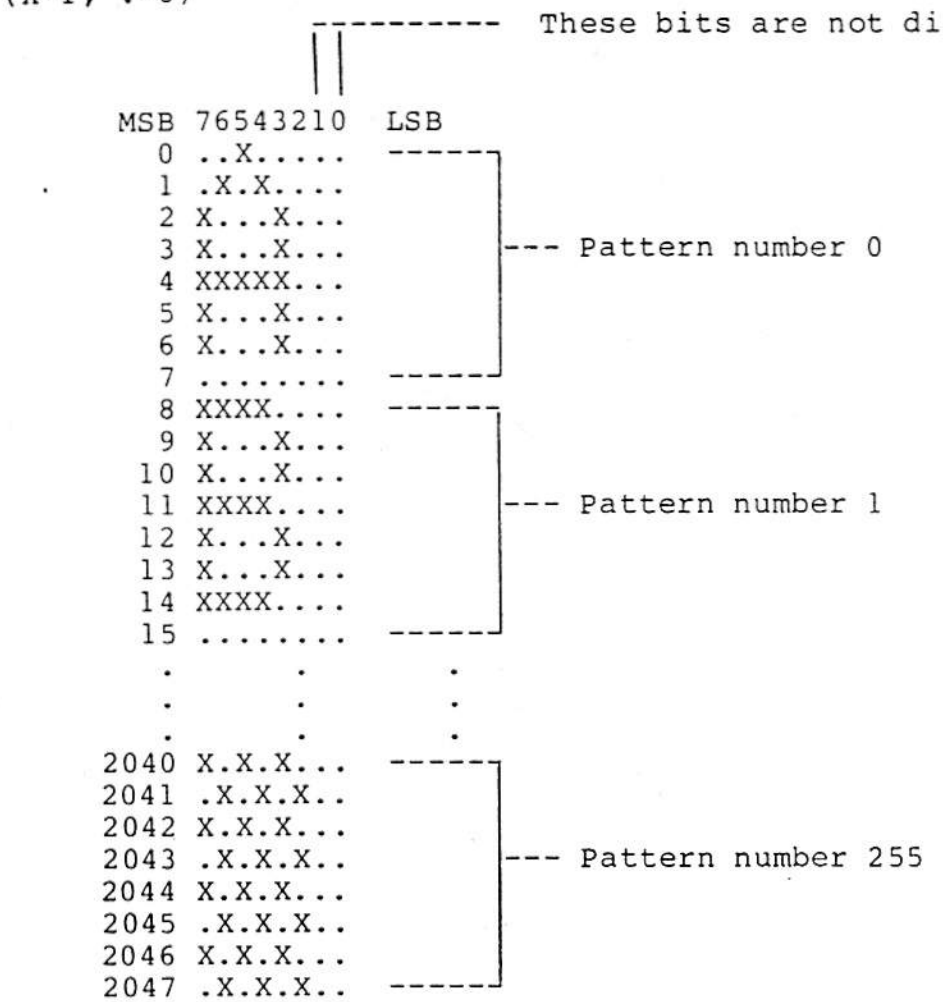
2. Pattern Generator Table Settings

- The pattern generator table is an area that stores the pattern fonts.
- Each pattern has a number from PN0 and PN255.
- The font for each pattern is constructed from 8 bytes, and the lower two bits of each of the eight bytes is not displayed.
- Set the beginning (head) address of the pattern generator table in register R#4.

	MSB 7	6	5	4	3	2	1	0 LSB	
R#4	0	0	A16	A15	A14	A13	A12	A10	Pattern generator table base address register

Pattern Generator Table

(X=1, .=0)



3. Pattern Name Table Settings

- The pattern name table is composed of one byte for each screen pattern. Each byte specifies a unique pattern.
- Set the beginning (head) address of the pattern name table in register R#2.

	MSB 7	6	5	4	3	2	1	0	LSB
R#2	0	A16	A15	A14	A13	A12	A10	A9	Pattern name table base address register

Pattern Name Table

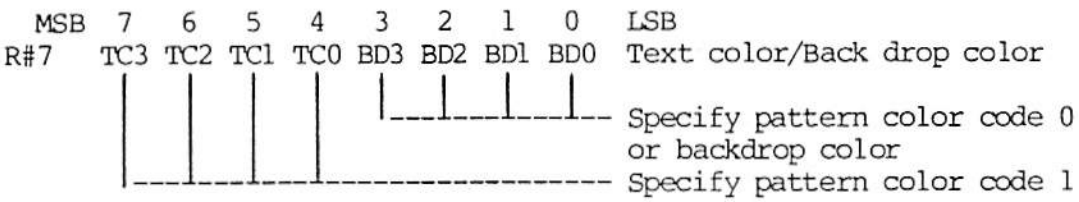
	Base address
(0, 0)	0
(1, 0)	1
(2, 0)	2
	.
	.
	.
(39, 0)	39
(0, 1)	40
	.
	.
	.
(39,23)	959 (byte)

	0	1	2	3	.	.	39	X
0	0	1	2	3	.	.	39	
1	40	41	42	43	.	.	79	
.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	
22	880	881	.	.	.	.	919	
23	920	921	.	.	.	.	959	

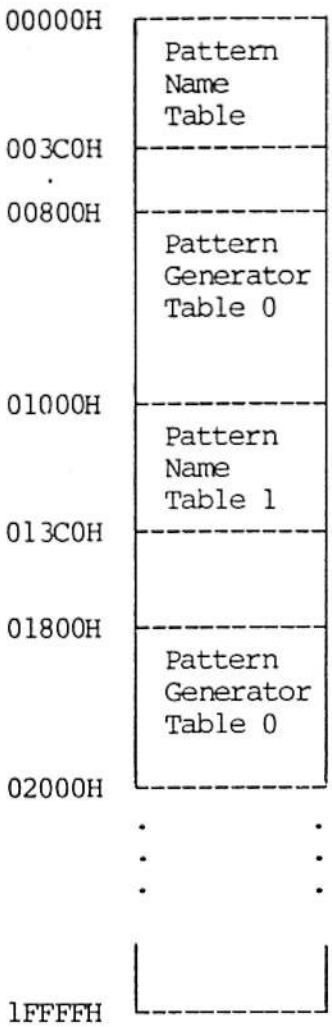
Y

Screen display correspondence

4. Color Register Settings



Example of VRAM allocation in TEXT 1 mode



	MSB	7	6	5	4	3	2	1	0	LSB
R#2		0	0	0	0	0	0	0	0	
			A16	A15	A14	A13	A12	A11	A10	

	MSB	7	6	5	4	3	2	1	0	LSB
R#4		0	0	0	0	0	0	0	1	
				A16	A15	A14	A13	A12	A11	

	MSB	7	6	5	4	3	2	1	0	LSB
R#2		0	0	0	0	0	1	0	0	
			A16	A15	A14	A13	A12	A11	A10	

	MSB	7	6	5	4	3	2	1	0	LSB
R#4		0	0	0	0	0	0	1	1	
				A16	A15	A14	A13	A12	A11	

A maximum of 32 pages may be allocated in the same manner (using a 128K-byte VRAM)

TEXT 2 MODE

Characteristics

- Pattern size	6 dots (w) x 8 dots (h)
- Patterns	256 types
- Screen pattern count	80 (w) x 24 (h) patterns 80 (w) x 26.5 (h) patterns
- Pattern blinking	Possible for each character
- Pattern colors	Two colors out of 512 colors (per screen), four if using blinking
- VRAM area per screen	8K bytes

Controls

- Pattern font	VRAM pattern generator table
- Screen pattern location	VRAM pattern name table
- Blink attributes	VRAM color table
- Pattern color code 1	High-order four bits of R#7
- Pattern color code 0	Low-order four bits of R#7
- Background color code	Low-order four bits of R#7
- . Pattern color code 1	High-order four bits of R#12 (Used for blinking)
- Pattern color code 0	Low-order four bits of R#12 (Used for blinking)

Initial Settings

1. Mode and Register Settings

	MSB 7	6	5	4	3	2	1	0 LSB	
R#0	0	DG	IE2	IE1	0*	1*	0*	0	Mode register 0
R#1	0	BL	IE0	1*	0*	0	SI	MAG	Mode register 1
R#8	MS	LP	TP	CB	VR	0	SP	BW	Mode register 2
R#9	LN	0	S1	S0	IL	EO	NT	DC	Mode register 3

* Example of settings in TEXT 2 mode
In this display mode, if LN is set to 1, 26.5 lines are selected, and if LN is set to 0, 24 lines are selected. All other bits are set accordingly

2. Pattern Generator Table Settings

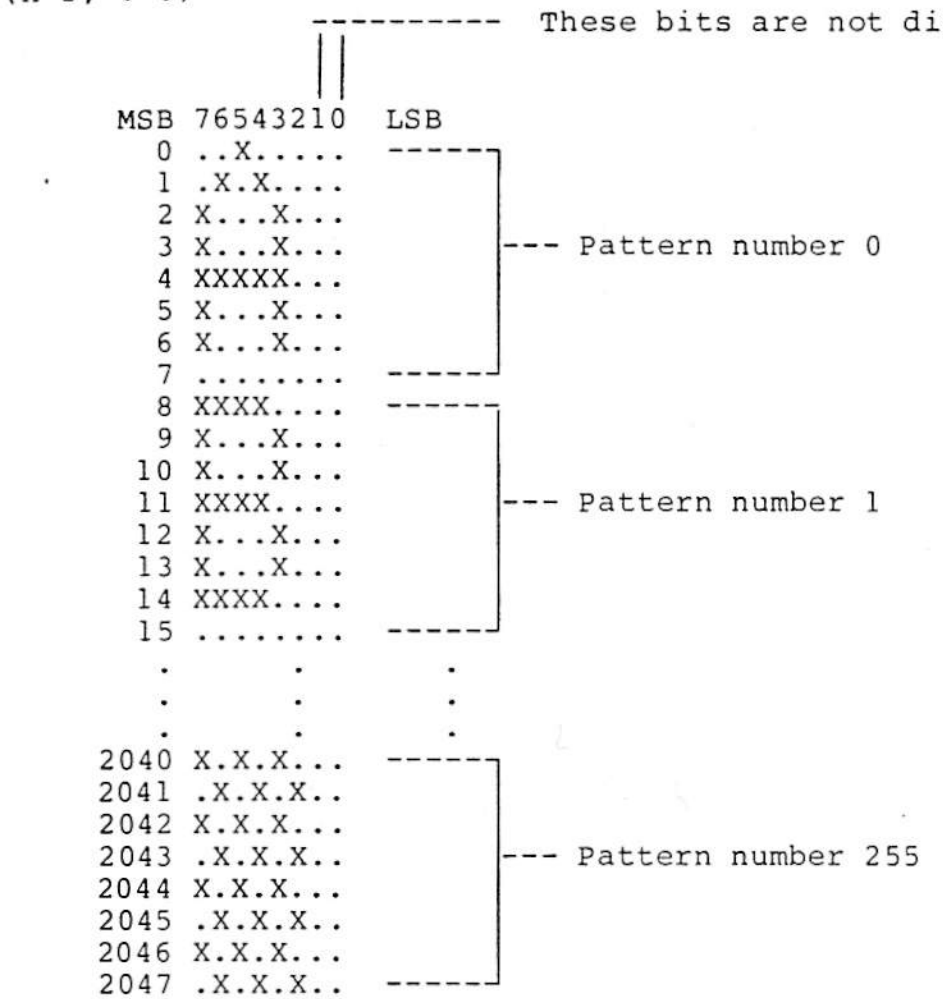
- The pattern generator table is an area that stores the pattern fonts.
- Each pattern has a number from PN0 to PN255.
- Set the beginning (head) address of the pattern generator table in register R#4.

	MSB 7	6	5	4	3	2	1	0 LSB	
R#4	0	0	A16	A15	A14	A13	A12	A11	Pattern generator table base address register

- The font for each pattern is constructed from 8 bytes, and the lower two bits of each of eight bytes is not displayed.

Pattern Generator Table

(X=1, .=0)



3. Pattern Name Table Settings

- The pattern name table is composed of one byte for each screen pattern. Each byte specifies a unique pattern.
- If LN is set to 0, the screen display pattern is 80 (w) x 24 (h); and if LN is set to 1, the screen display pattern is 80 (w) x 26.5 (h). The upper half of the 27th pattern (h) is displayed.
- Set the beginning (head) address of the pattern name table in register R#2.

	MSB 7	6	5	4	3	2	1	0 LSB	
R#2	0	A16	A15	A14	A13	A12	A11	A10	Pattern generator table base address register

Pattern Name Table

	Base address
(0, 0)	0
(1, 0)	1
(2, 0)	2
	.
	.
	.
(79, 0)	79
(0, 1)	80
	.
	.
	.
(79,26)	2159

```
     0   1   2   3   .   .   39   X
0    0   1   2   3   .   .   39
1   40  41  42  43   .   .   79
 .   .   .   .   .   .   .   .
 .   .   .   .   .   .   .   .
25 2000 2001 .   .   .   . 2079
26 2080 2081 .   .   .   . 2159
 Y
```

Screen display correspondence

4. Color Table Settings

- In TEXT 2 mode, each pattern has one bit apiece for the attribute area, and if this bit is set to 1, the pattern blink attribute will be set.
- Set the beginning (head) address of the color table in registers R#3 and R#10.

	MSB 7	6	5	4	3	2	1	0	LSB
R#3	A13	A12	A11	A10	A9	1	1	1	
R#10	0	0	0	0	0	A16	A15	A14	Color table base address register

Color Table

MSB	7	6	5	4	3	2	1	0	LSB
0	(0, 0)	(1, 0)	(2, 0)	(3, 0)	(4, 0)	(5, 0)	(6, 0)	(7, 0)	
1	(8, 0)	) 9, 0)	(10, 0)	(10, 0)	(11, 0)	(12, 0)	(13, 0)	(14, 0)	
.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	
269	(72,26)	.	.	.	.	.	.	(79,26)	

5. Color Register Settings

- Set the color for pattern 1 in the high-order bits of register R#7.
- Set the color for pattern 0 in the low-order bits of register R#7.

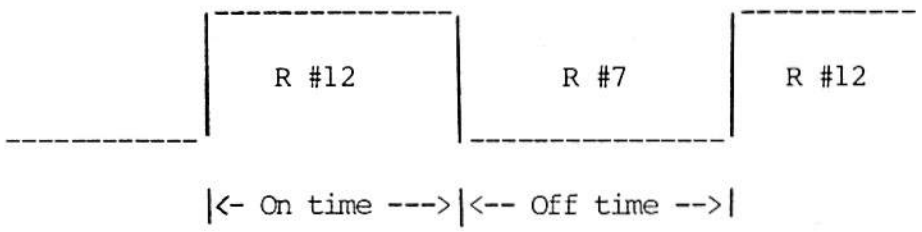
	MSB 7	6	5	4	3	2	1	0	LSB
R#7	TC3	TC2	TC1	TC0	BD3	BD2	BD1	BD0	Text color/ Back drop color

- Set the blink attribute for the corresponding pattern by setting an alternate color code in register R#12. The pattern will be blinked by using the color codes set in registers R#7 and R#12.

	MSB 7	6	5	4	3	2	1	0	LSB
R#12	TC3	TC2	TC1	TC0	BD3	BD2	BD1	BD0	Text color/ Back drop color

6. Blink Register Settings

- The color codes set in registers R#7 and R#12 will be alternately dsplayed for blinking; however, the blinking period attribute (time on and time off) can also be set in register R#13.

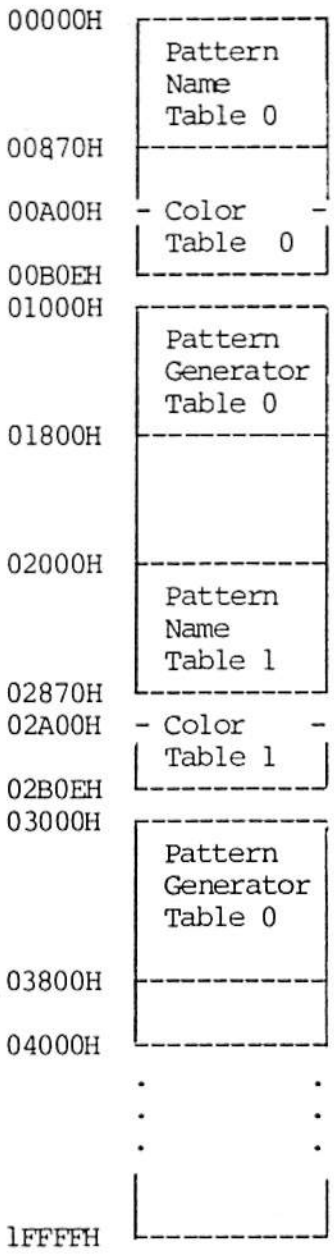


	MSB 7	6	5	4	3	2	1	0	LSB
R#13	ON3	ON2	ON1	ON0	OF3	OF2	OF1	OF0	Blinking period register

- The data for the ON and OFF times are shown below at NTSC mode.

DATA (Binary)	TIME (ms)
0 0 0 0	0
0 0 0 1	166.9
0 0 1 0	333.8
0 0 1 1	500.6
0 1 0 0	667.5
0 1 0 1	834.4
0 1 1 0	1001.3
0 1 1 1	1168.2
1 0 0 0	1335.1
1 0 0 1	1501.9
1 0 1 0	1668.8
1 0 1 1	1835.7
1 1 0 0	2002.6
1 1 0 1	2169.5
1 1 1 0	2336.3
1 1 1 1	2503.2

Example of VRAM allocation in TEXT 2 mode



Pattern name table base address

	MSB	7	6	5	4	3	2	1	0	LSB
R#2		0	0	0	0	0	0	0	0	
			A16	A15	A14	A13	A12	A11	A10	

Color table base address

	MSB	7	6	5	4	3	2	1	0	LSB
R#3		0	0	1	0	1	1	1	1	
		A13	A12	A11	A10	A9				
R#10		0	0	0	0	0	0	0	0	
							A16	A15	A14	

Pattern generator table base address

	MSB	7	6	5	4	3	2	1	0	LSB
R#4		0	0	0	0	0	0	1	1	
				A16	A15	A14	A13	A12	A11	

A maximum of 16 pages may be allocated in the same manner (using a 128K-byte VRAM)

GRAPHIC 1 MODE

Characteristics

- Pattern size	8 dots (w) x 8 dots (h)
- Patterns	256 types
- Screen pattern count	32 (w) x 24 (h) patterns
- Pattern colors	16 colors out of 512 colors (per screen)
- Sprite mode	Sprite mode 1
- VRAM area per screen	4K bytes

Controls

- Pattern font	VRAM pattern generator table
- Screen pattern location	VRAM pattern name table
- Pattern color codes 1 & 0	Can be specified as a group for each 8-pattern set, in the VRAM color table
- Background color code	Low-order four bits of R#7
- Sprites	VRAM sprite attribute table, VRAM sprite pattern table

Initial Settings

1. Mode and Register Settings

	MSB 7	6	5	4	3	2	1	0 LSB	
R#0	0	DG	IE2	IE1	0*	0*	0*	0	Mode register 0
R#1	0	BL	IE0	0*	0*	0	SI	MAG	Mode register 1
R#8	MS	LP	TP	CB	VR	0	SP	BW	Mode register 2
R#9	0	0	S1	S0	IL	EO	NT	DC	Mode register 3

* Examples of settings in GRAPHIC 1 mode

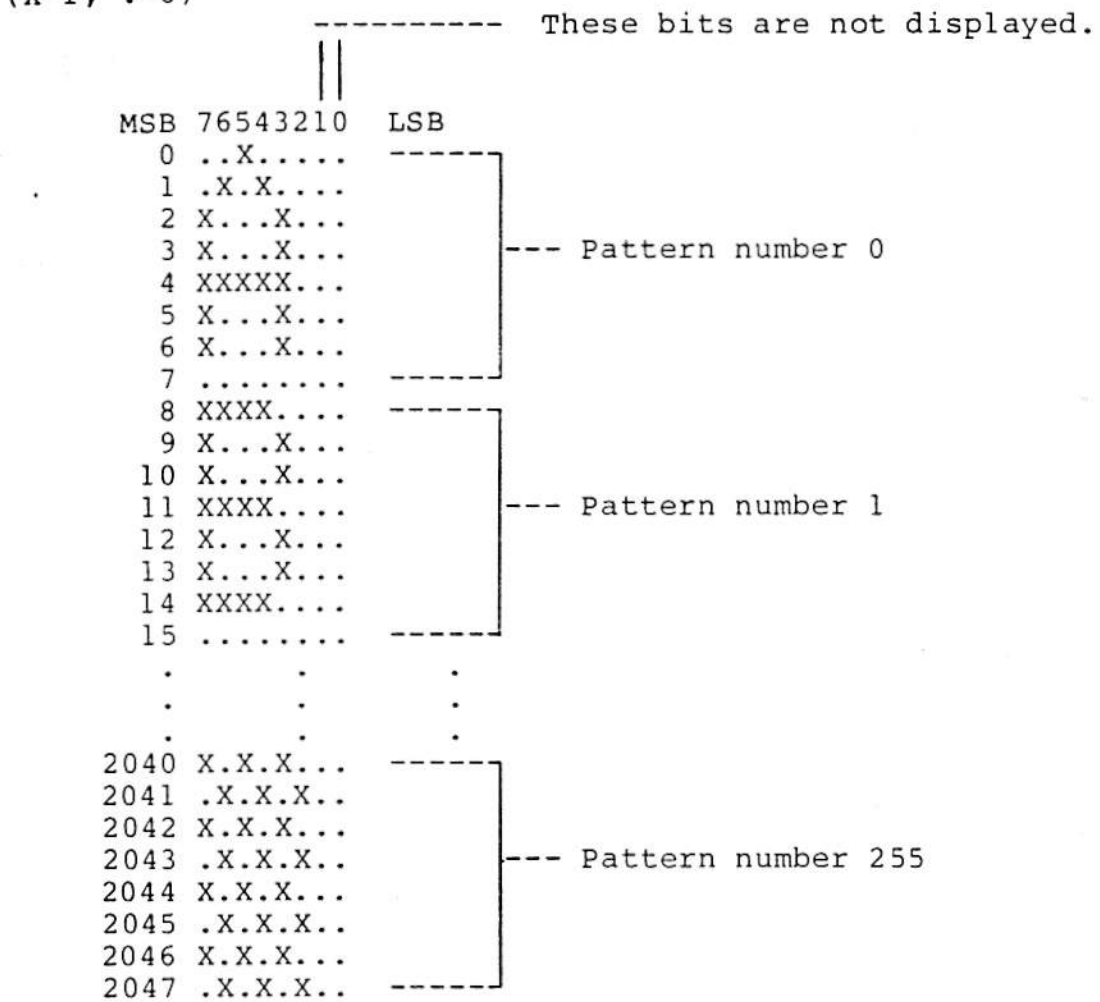
2. Pattern Generator Table Settings

- The pattern generator table is an area that stores the pattern fonts.
- Each pattern has a number from PN0 to PN255.
- The font for each pattern is constructed from 8 bytes.
- Set the beginning (head) address of the pattern generator table in register R#4.

	MSB 7	6	5	4	3	2	1	0 LSB	
R#4	0	0	A16	A15	A14	A13	A12	A11	Pattern generator table base address register

Pattern Generator Table

(X=1, .=0)

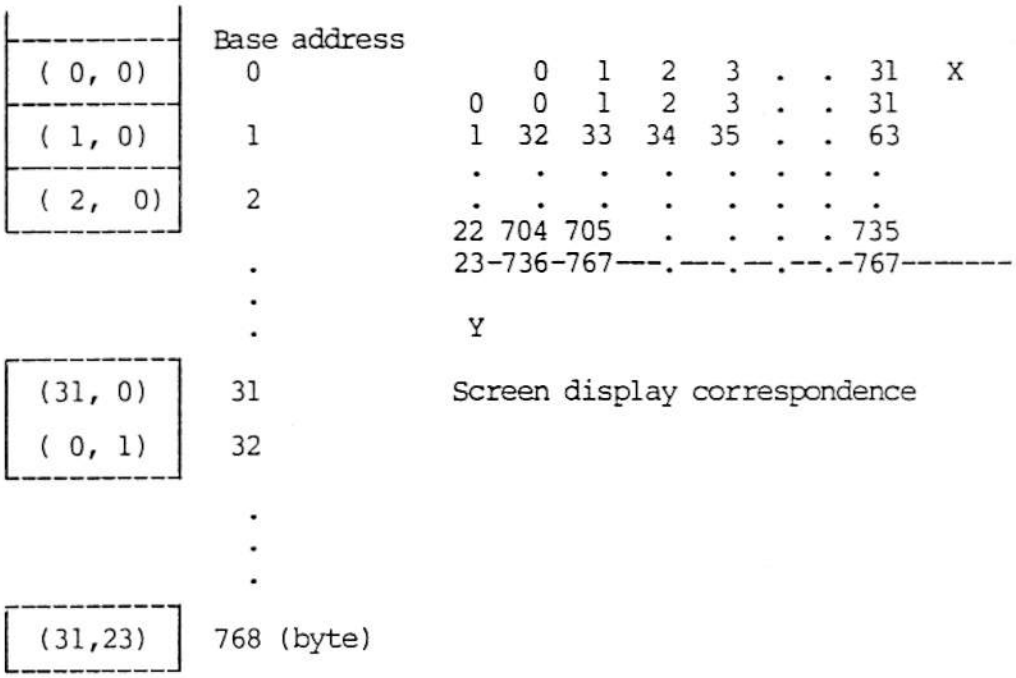


3. Pattern Name Table Settings

- The pattern name table is composed of one byte for each screen pattern. Each byte specifies a unique pattern.
- Set the beginning (head) address of the pattern name table in register R#2.

	MSB 7	6	5	4	3	2	1	0 LSB	
R#2	0	A16	A15	A14	A13	A12	A11	A10	Pattern generator table base address register

Pattern Name Table



4. Color Register Settings

	MSB 7	6	5	4	3	2	1	0	LSB
R#7	TC3	TC2	TC1	TC0	BD3	BD2	BD1	BD0	Text color/Back drop color register
									Specify backdrop color code
									Ignored

5. Color Table Settings

- The colors for pattern color 1 and pattern color 0 are set in groups of 8 patterns.
- Set the beginning (head) address of the color table in registers R#3 and R#10.

	MSB 7	6	5	4	3	2	1	0	LSB
R#3	A13	A12	A11	A10	A9	A8	A7	A6	Color table base
R#11	0	0	0	0	0	A16	A15	A14	address register

Color Table

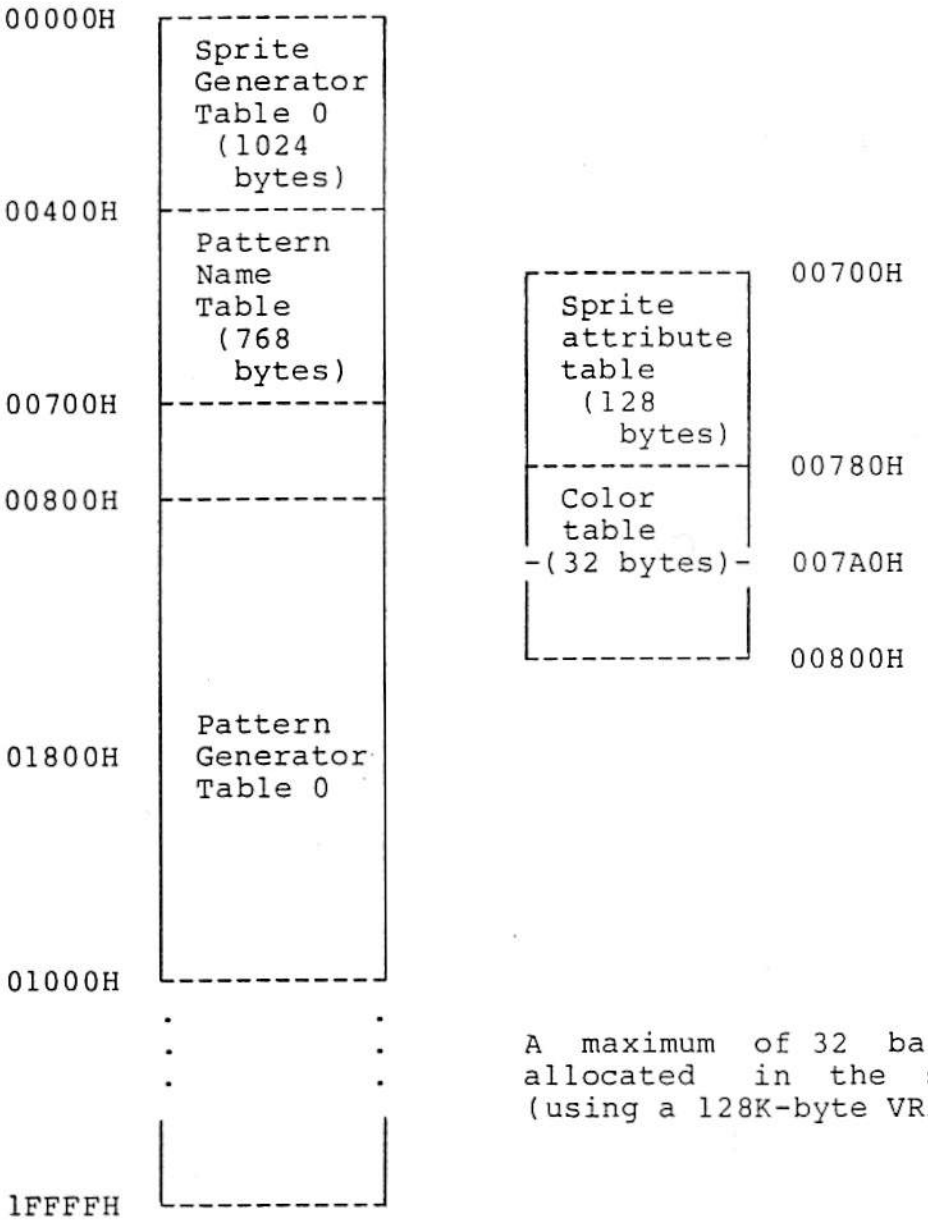
	MSB 7	6	5	4	3	2	1	0	LSB
0	FC3	FC2	FC1	FC0	BC3	BC2	BC1	BC0	Pattern Nos. 0 to 7
1	FC3	FC2	FC1	FC0	BC3	BC2	BC1	BC0	Pattern Nos. 8 to 15
.	.	.	.	.	.	.	.	.	. . . .
32	FC3	FC2	FC1	FC0	BC3	BC2	BC1	BC0	Pattern Nos. 248 to 255

6. Sprite Settings

- Set the beginning (head) address of the sprite attribute table in registers R#5 and R#11; and set the beginning (head) address of the sprite pattern generator table in register R#6. For details about sprites, see the section on SPRITE MODE 1.

	MSB 7	6	5	4	3	2	1	0 LSB	
R#5	A14	A13	A12	A11	A10	A9	A8	A7	Sprite attribute table
R#11	0	0	0	0	0	0	A16	A15	base address register
R#6	0	0	A16	A15	A14	A12	A11	A10	Sprite pattern generator table base address register

Example of VRAM allocation in GRAPHIC 1 mode



A maximum of 32 bages may be allocated in the same manner (using a 128K-byte VRAM)

GRAPHIC 2 AND GRAPHIC 3 MODES

The GRAPHIC 2 and GRAPHIC 3 modes are identical except for the handling of sprites.

Characteristics

- Pattern size	8 dots (w) x 8 dots (h)
- Patterns	768 types
- Screen pattern count	32 (w) x 24 (h) patterns
- Pattern colors	16 colors out of 512 colors (per screen)
- Sprite mode	Sprite mode 1 (GRAPHIC 2) Sprite mode 2 (GRAPHIC 3)
- VRAM area per screen	16K bytes

Controls

- Pattern font	VRAM pattern generator table
- Screen pattern location	VRAM pattern name table
- Pattern color codes 1 & 0	Can be specified as a group for each raster, in the VRAM color table
- Background color code	Low-order four bits of R#7
- Sprites	VRAM sprite attribute table, VRAM sprite pattern table

Initial Settings

1. Mode and Register Settings

	MSB 7	6	5	4	3	2	1	0 LSB	
R#0	0	-	IE2	IE1	0*	%*	%*	0	Mode register 0
						|	|		
						|	|-------		0, 1 for GRAPHIC 2 mode
						|----------			1, 0 for GRAPHIC 3 mode
R#1	0	BL	IE0	0*	0*	0	SI	MAG	Mode register 1
R#8	MS	LP	TP	CB	VR	0	SP	BW	Mode register 2
R#9	0	0	S1	S0	IL	EO	NT	DC	Mode register 3

* Examples of settings in GRAPHIC 2 mode or GRAPHIC 3 mode

All other bits are set accordingly

2. Pattern Generator Table Settings

- The pattern generator table is an area that stores the pattern fonts.
- Each pattern group has a number from PN0 to PN255; and since each group may have three members, 768 patterns may be specified.
- The font for each pattern is constructed from 8 bytes.
- Set the beginning (head) address of the pattern generator table in register R#4.cwl2

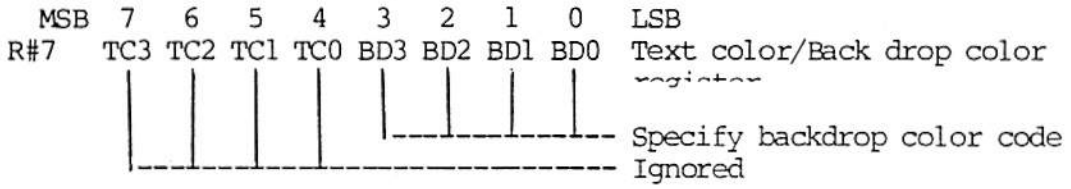
	MSB	7	6	5	4	3	2	1	0	LSB	
R#4		0	0	A16	A15	A14	A13	1	1	Pattern generator table base address register	

3. Color Table Settings

- The colors for pattern color 1 and pattern color 0 are set in groups of 1 raster.
- The color table corresponds to the pattern generator table on a one-to-one basis.
- Set the beginning (head) address of the color table in registers R#3 and R#10.

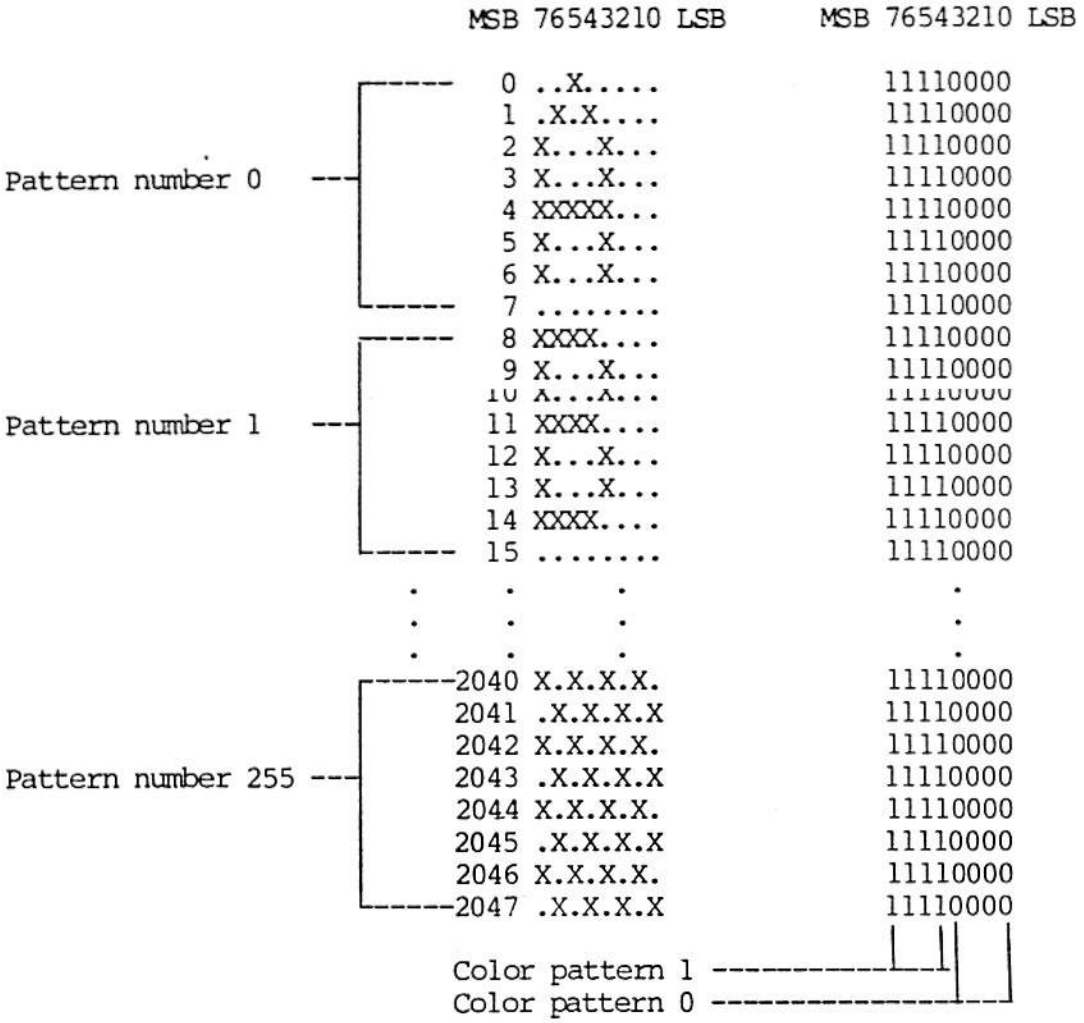
	MSB	7	6	5	4	3	2	1	0	LSB	
R#3		A13	1	1	1	1	1	1	1	Color table base address register	
R#11		0	0	0	0	0	A16	A15	A14		

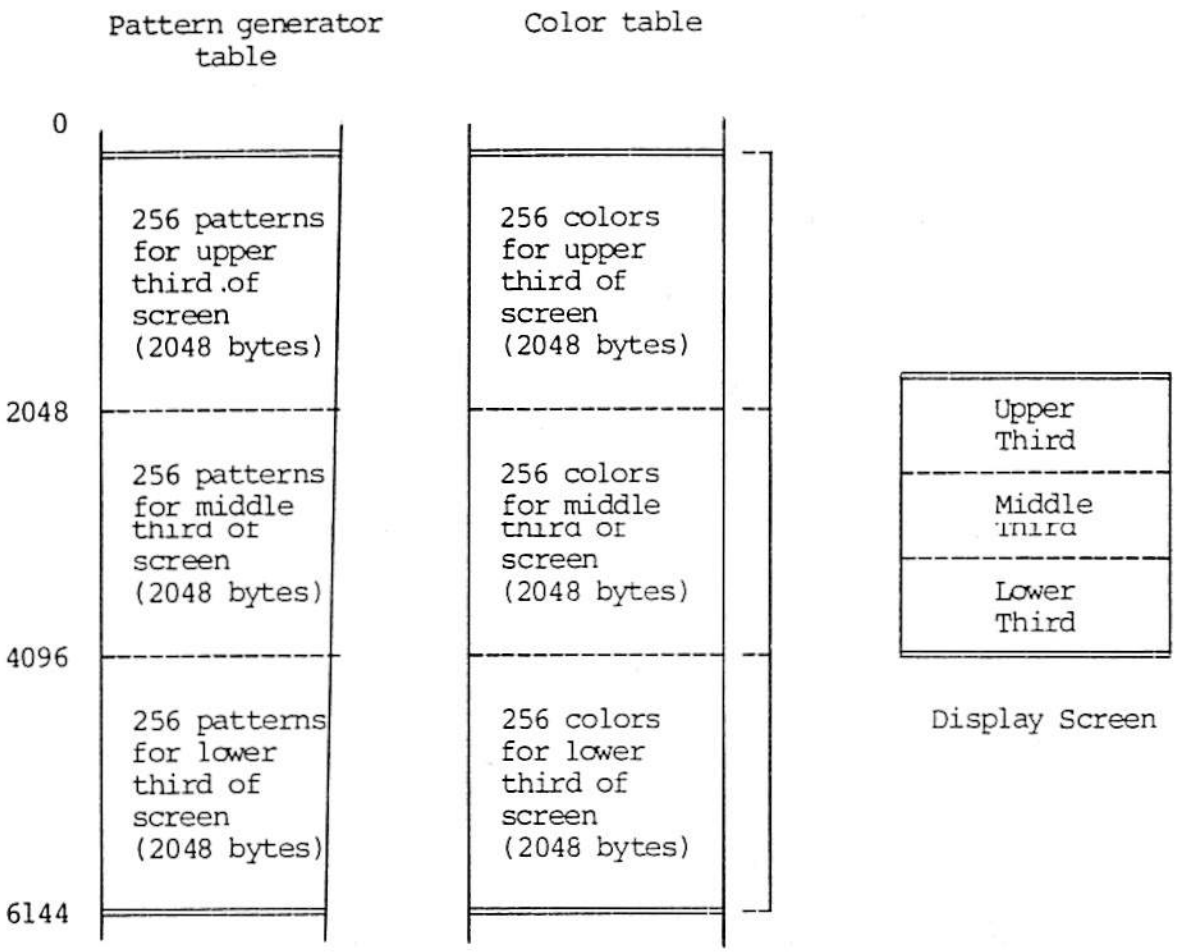
4. Color Register Settings



Pattern Generator Table

(X=1, .=0)





3. Pattern Name Table Settings

- The pattern name table is composed of one byte for each screen pattern. Each byte specifies a unique pattern.
  The upper, middle, and lower parts of the screen are treated as three parts for a total of 768 patterns.

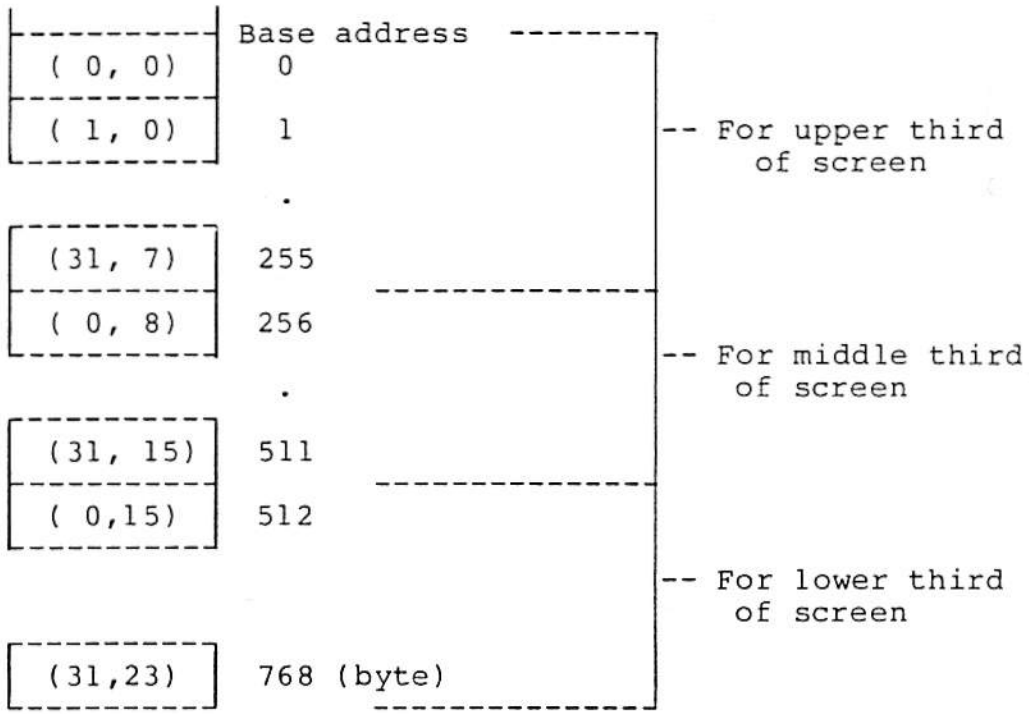
Pattern Name Table

(0, 0)	Pattern display area for upper third of screen (256 bytes)	(31, 0)
(0, 7)		(31, 7)
(0, 8)	Pattern display area for middle third of screen (256 bytes)	(31, 8)
(0,15)		(31,15)
(0,16)	Pattern display area for lower third of screen (256 bytes)	(31,16)
(0,23)		(31,23)

- Set the beginning (head) address of the pattern name table in register R#2.

	MSB 7	6	5	4	3	2	1	0 LSB	
R#2	0	A16	A15	A14	A13	A12	A11	A10	Pattern name table base address register

Pattern Name Table

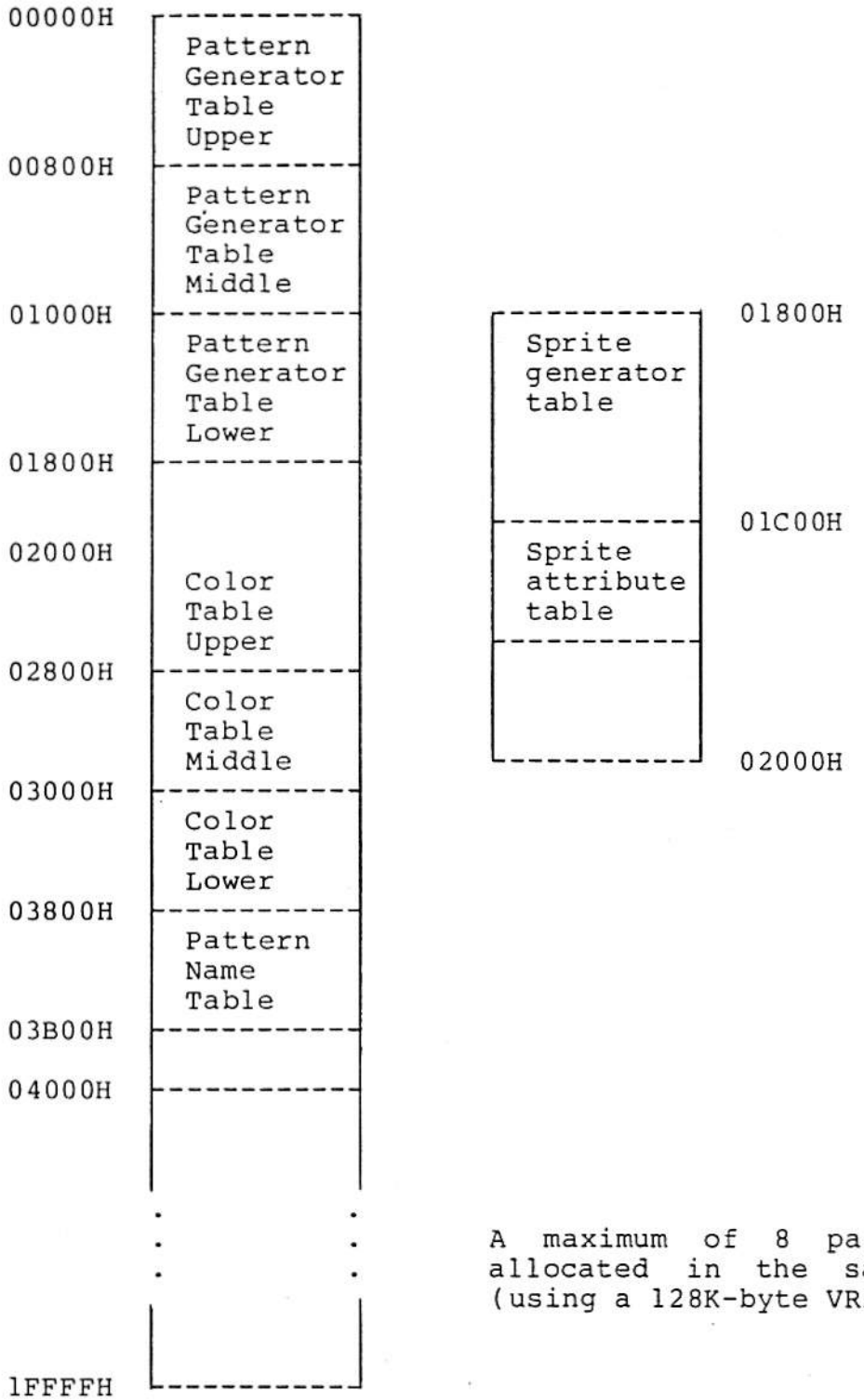


6. Sprite Settings

- Set the beginning (head) address of the sprite attribute table in registers R#5 and R#11; and set the beginning (head) address of the sprite pattern generator table in register R#6. For details about sprites pertaining to GRAPHIC 1 mode, see the page on SPRITE MODE 1, and for details about sprites pertaining to GRAPHIC 2 mode, see the page on SPRITE MODE 2.

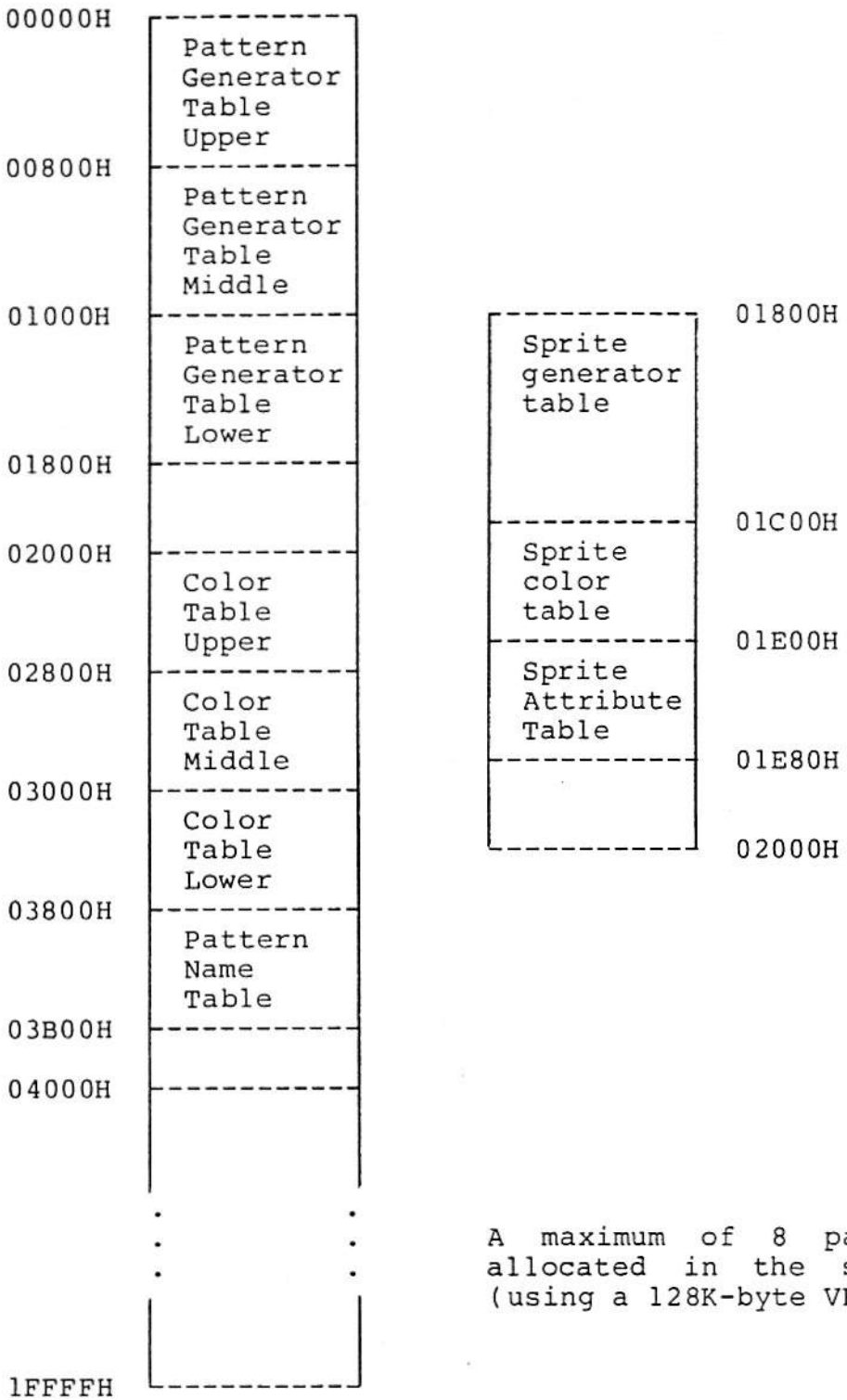
	MSB 7	6	5	4	3	2	1	0 LSB	
R#5	A14	A13	A12	A11	A10	A9	A8	A7	Sprite attribute table
R#11	0	0	0	0	0	0	A16	A15	base address register
R#6	0	0	A16	A15	A14	A12	A11	A10	Sprite pattern generator table base address register

Example of VRAM allocation in GRAPHIC 2 mode



A maximum of 8 pages may be allocated in the same manner (using a 128K-byte VRAM)

Example of VRAM allocation in GRAPHIC 3 mode



A maximum of 8 pages may be allocated in the same manner (using a 128K-byte VRAM)

1.6 PROGRAMMABLE SOUND GENERATOR AY-3-8910

The AY-3-8910 is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through its 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through its 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

SOUND GENERATING BLOCK

The Basic Blocks in the PSG which produce the programmed sounds include:

Tone Generators

Produce the basic square wave tone frequencies for each channel (A, B, C).

Noise Generator

Produce a frequency modulated pseudo random pulse width square wave output.

Mixers

Combine the outputs of the Tone Generators and the Noise Generator. 1 for each channel (A, B, C).

Amplitude Control

Provides the D/A connectors with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator.

Envelope Generator

Produces an envelope pattern which can be used to amplitude modulate the output of each mixer.

D/A Converters

The 3 D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control.

Since virtually all uses of microprocessor-based sound would require interfacing between the outside world and the processor, 2 I/O ports (A and B) has been included in the PSG.

To output data from the CPU bus to a peripheral device connected to I/O port A would require only the following steps:

1. Latch address R7 (select $\overline{\text{Enable}}$ register)

2. Write data to PSG (setting B6 of R7 to "1")

3. Latch address R16 (select IOA register)

4. Write data to PSG (data to be output on I/O port A)

To input data from I/O port A to the CPU bus would require the following:

1. Latch address R7 (select $\overline{\text{Enable}}$ register)

2. Write data to PSG (select B6 to R7 to "0")

3. Latch address R16 (select IOA register)

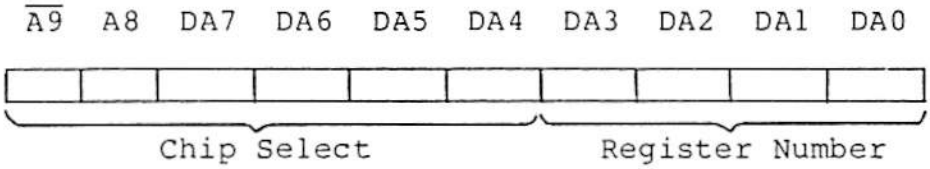
4. Read data from PSG (data from I/O port A)

To do input/output on I/O port B, use Register 17, instead of Register 16. Note that once loaded with data in the input mode, the data will remain on the I/O ports until changed either by loading different data, by applying a reset (grounding the Reset Pin), or by switching to the input mode.

DA7-DA0 (input/output/high impendance): Pins 30-37

Data Address 7-0

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the data mode, DA7-DA0 correspond to Register Array bits B7-B0. In the address mode, DA3-DA0 select the register #(0-17) and DA7-DA4 in conjunction with address input A9 and A8 form the high order address (chip select).



A8 (input) : Pin 25

$\overline{A9}$ (input) : Pin 24

$\overline{\text{Address 9}}$, Address B

These "extra" address bits are made available to enable the positioning of the PSG (assignment a 16 word memory space) in a total 1024 word memory area rather than in a 256 word memory area as defined by address bits DA7-DA0 alone. If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down (A9) or pull-up (A8) resistor. In SVI-728, A9 and A8 are tied to an external ground and +5V respectively.

$\overline{\text{RESET}}$ (input) : Pin 23

For initialization/power-on purpose, applying a logic "0" (ground) to the Reset Pin will reset all registers to "0". The Reset Pin is provided with an on-chip pull-up resistor.

CLOCK (input): Pin 22

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators.

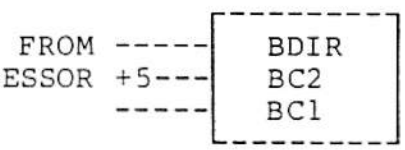
BDIR, BC2, BCl (inputs) : Pins 27, 28, 29

Bus DIRection, Bus Control 2, 1

These bus control signals are generated directly by Z80A series of microprocessors to control all external and internal bus operations in the PSG. When using a processor other than the Z80A, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the processor.

This could simplify the programming of the bus control signals to the following, which would only require that the processor generate 2 bus control signals (BDIR and BC1, with BC2 tied to +5V):

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE.
0	1	1	READ FRIN PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS



ANALOG CHANNEL A, B, C (output)

Each of these signals is the output of its corresponding mix of T4, and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7 - IOA0 (input/output) : Pins 14 - 21
IOB7 - IOB0 (input/output) : Pins 6 - 13

Input/Output A7-A0, B7-B0

Each of these 2 parallel input/output ports provides 8 bits of parallel data to/from the PSG/CPU bus from/to any external devices connected to the IOA or IOB pins. Each pin is provided with an on-chip pull-up resistor, so that when in the "input" mode, all pins will read normally high. Therefore, the recommended method for scanning external switches, for example, would be to ground the input bit.

TEST 1 : Pin 39
TEST 2 : Pin 26

These pins are for user test purposes only and should be left open - do not use a tie-points.

Vcc : Pin 40

Nominal +5 Volt power supply to the PSG.

Vss : Pin 1

Ground reference for the PSG.

The Programmable Sound Generator

The PSG AY-3-8910 generates all required sound under software control. There are 2 8-bit I/O ports which are programmed as follow:

Port A : Programmed as input port and is used for the input signal from 2 joysticks controllers.

Port B : Programmed as output port.

Detail signals for the ports are listed in the table below:

AY-3-8910 I/O Port A (Input Port)

```
D0 ------ Forwared*
D1 ------ Backward*
D2 ------ Left*
D3 ------ Right*
D4 ------ TRGA1*
D5 ------ TRGA2*
D6 ------ NC
D7 ------ Cassette Tape Read

* Used by Joystick 1 when bit 6 of Port B is low
  Used by Joystick 2 when bit 6 of Port B is high
```

AY-3-8910 I/O Port (Output Port)

```
D0 -- )
D1 -- ) Make the "H" level, when used as an output port
D2 -- ) Tied an open collector buffer to the output
D3 -- )
D4 --   O/P
D5 --   O/P
D6 --   Input Select
D7 --   NC
```

1.7 PROGRAMMABLE PERIPHERAL INTERFACE

Inside the X'PRESS, there are two customised Integraded Chips, ULA5RA08T and ULA9RA041, to strobe the keyboard line, to select slots and memory expansion and to control the cassette tape system. The ports are programmed as follows:

Port A : Programmed as output port. Bits 0-7 are the address slots select signals that choose the slots to be used.

Port B : Programmed as output port and is used for keyboard read data.

Port C : Programmed as output port. Bits 0-3 outputs BCD data for keyboard scanning. Bits 4-6 outputs control signals for the cassette. Bit 7 is used to mix PSG sound data.

The functional configuration of the PPI is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the ULA9RA041 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control buses in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the ULA and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the ULA to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the ULA.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the ULA.

(A0 and A1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of 1 of the 3 ports or the control word registers. They are normally connected to the least significant bits of the address bus (A0 and A1)

Basic Operation

A	A	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A ====== DATA BUS
0	1	0	1	0	PORT B ====== DATA BUS
1	0	0	1	0	PORT C ====== DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS ====== PORT A
0	0	0	1	0	DATA BUS ====== PORT B
0	1	0	1	0	DATA BUS ====== PORT C
1	0	0	1	0	DATA BUS ====== CONTROL
					OUTPUT OPERATION (WRITE)
X	X	X	X	1	DATA BUS ====== 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS ====== 3-STATE

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the ULAs. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the ULAs.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)
Control Group B - Port B and Port C lower (C3 - C0)

The Control Word Register can only be written into. No Read operation of the Control Word Register is allowed.

Port A, B and C

The PPI contains three 8-bit ports (A, B and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the PPI.

Port A. 1 8-bit data output latch/buffer and 1 8-bit data input latch.

Port B. 1 8-bit data input/output latch/buffer and 1 8-bit data input buffer.

Port C. 1 8-bit data output latch/buffer and 1 8-bit data input buffer (no latch for input). This port can be dividied into 2 4-bit port under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

Mode Selection

There are 3 basic modes of operation that can be selected by the system software.

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode (i.e. all 24 lines will be in the high impendance state). After the reset is removed, the ULA can remain in the input mode with no additional initialization required. During the execution of the system programme, any of the other modes may be selected using a signle output instruction. This allows the ULA to serve a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into 2 portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seen confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the ULAs has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the 8 bits Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the PPI is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable
(BIT-RESET) - INTE is RESET - Interrupt enable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

PPI Port A (Input Port)

D0 ------) 0000 - 3FFF address slot select signal
D1 ------)
D2 ------) 4000 - 7FFF address slot select signal
D3 ------)
D4 ------) 8000 - BFFF address slot select signal
D5 ------)
D6 ------) C000 - FFFF address slot select signal
D7 ------)

PPI Port B (Input Port)

D0 - D7 ------ Keyboard Read Data

PPI Port C (Output Port)

D0 - D3 ------ Keyboard BCD Output Data
(For Keyboard Scanning)
D4 ------ Cassette Motor On
(0= Motor On, 1 = Motor Off)
D5 ------ Cassette Write Data
D6 ------ Cassette Audio Control
(1 = Enable other channel in)
(0 = Disable other channel in)
D7 ------ Mix PSG Sound Data

PPI Control Word (Write Only)

Initial Set	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	1	0	0	1	0

1.8 FLOPPY DISK CONTROLLER DESCRIPTION

Functional Description

The Floppy Disk Formatter block diagram (STM-003-C). The primary sections include the Parallel Processor Interface and the Floppy Disk Interface.

DATA SHIFT REGISTER - This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

DATA REGISTER - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

TRACK REGISTER - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

SECTOR REGISTER (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

COMMAND REGISTER (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

STATUS REGISTER (STR) - This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register cab be read onto the DAL, but not loaded from the DAL.

CRC LOGIC - This logic is used to check or to generate the 16-bit Cycle Redundancy Check (CRC). The polynominal is:

$$G(x) = X^{16} + x^{12} + x^{5} + 1$$

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is present to ones prior to data being shifted through the circuit.

ARITHMETIC/LOGIC UNIT (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modificaiton and comparisons with the disk recorded ID field.

TIMING AND CONTROL - All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has 2 different modes of operation according to th state of DDEN. When DDEN = 0, double density (MFD) is assumed. When DDEN = 1, single density (FM) is assumed.

AM DETECTOR - The address mark detector detects ID, data and index address marks during read and write operations.

Whenever a Read or Write command (Type II or III) is received FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the 8 Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1793. The DAL are 3 state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read after 1 or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force interrupt command condition is met.

FLOPPY DISK INTERFACE

The 1793 has 2 modes of operation according to the state of DDEN (Pin 37). When DDEN = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1". For MFM formats, DDEN should be placed to a logical "0". Sector lengths are determined at format time by a special byte in the "ID" field. If this sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179 is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179 is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations, the FD1793 requires RAW READ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read Clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD1793 must find an address mark within the next 10 bytes, otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD1793 is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD1793 must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the VFOE (Pin 33) is provided for phase lock loop synchronization. VFOE will be active when:

(a) Both HLT and HLD are True

(b) Setting Time, if programmed, has expired

(c) The 1793 is inspecting data off the disk

If WF/VFOE is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1793 before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1793 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD1793 provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM (DDEN = 1) and 250 ns pulses in MFM (DDEN = 0). Write Data provides the unique address marks in both formats.

Also during write, 2 additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several 1 shots or delay lines which are located external to the FD1793. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

WRITE PRECOMPENSATION

Write precompensation (which counteracts the 'drifting' when flux transitions are placed close together on the more cramped inside tracks) is available to the user on any tracks that he feels necessary.

STATUS REGISTER SUMMARY

BIT	ALL TYPE 1 COMMANDS	READ ADDRESS	READ SECTOR
S7	Not Ready	Not Ready	Not Ready
S6	Write Protect	0	0
S5	Head Loaded	0	Record Type
S4	Seek Error	RNF	RNF
S3	CRC Error	CRC Error	CRC Error
S2	Track 0	Lost Data	Lost Data
S1	Index	DRQ	DRQ
S0	Busy	Busy	Busy

BIT	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	Not Ready	Not Ready	Not Ready
S6	0	Write Protect	Write Protect
S5	0	Write Fault	Write Fault
S4	0	RNF	0
S3	0	CRC Error	0
S2	Lost Data	Lost Data	Lost Data
S1	DRQ	DRQ	DRQ
S0	Busy	Busy	Busy

STATUS FOR TYPE 1 COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III commands will not execute unless the logically 'ored' with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S6	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK 00	When set, indicated Read/Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0	BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not used. On Read Track: Not used. On any Write: It indicates a Write Protect. This bit is reset whenupdated.
S5	RECORD TYPE/WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set command is under execution. When reset, no command is under execution.

CHAPTER 2

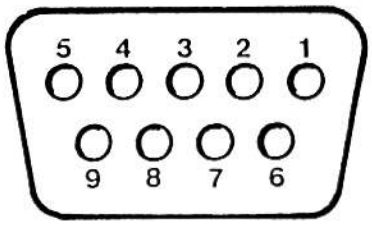
INPUT/OUTPUT SPECIFICATION

2.1 LIST OF CONNECTORS

PIN NAME	SPECIFICATION
1. Composite Video Output	RCA 2 pins connector
2. RF Modulated Signal	RCA 2 pins connector
Cassette	DIN 8 pins connector (DIN-45326)
I/O Port	AMP 9 pins connector
Printer	Amphenol 14 pins connector
Cartridge Bus	2.54 pace, 50 pins DGE connector for system expansion
Audio	RCA 2 pins connector
RS-232C Serial Interface	9 pins D-type connector (Female)
Optional Drive Expansion Slot	25 pins D-type connector (Female)
AC Power Input	AC power jack

2.3 INPUT/OUTPUT (JOYSTICK) PORTS

- SPECIFICATION — 8-bit parallel
- INPUT/OUTPUT — Input 4 bit, output 1 bit, bidirectional 2 bit per port
- LOGIC — Active high
- LEVEL — TTL
- CONNECTOR — AMP 9 pins compatible
- LIST OF PINS

PIN NO.	SIGNAL NAME	DIRECTION	PIN CONNECTION
1	FWD	INPUT	
2	BACK	INPUT	
3	LEFT	INPUT	
4	RIGHT	INPUT	
5	+5V*	--	
6	TRG 1	INPUT/ OUTPUT	
7	TRG 2	INPUT/ OUTPUT	
8	OUTPUT	OUTPUT	
9	GND	--	

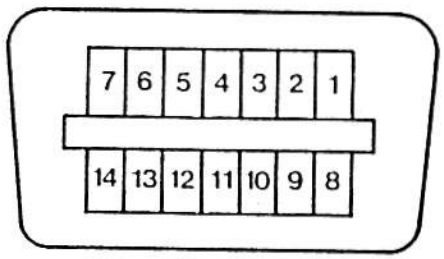
* Current capacity is 50mA

2.4 PRINTER INTERFACE

- SPECIFICATION — 8-bit parallel (modified centronics type)
- LEVEL — TTL
- CHARACTER CODE — Same to MSX display code
- CONNECTOR — AMP 14 pins compatible
- LIST OF PINS

PIN NO.	SIGNAL NAME
1	$\overline{\text{STB}}$
2	PDB0
3	PDB1
4	PDB2
5	PDB3
6	PDB4
7	PDB5
8	PDB6
9	PDB7
10	N.C.
11	BUSY
12	N.C.
13	N.C.
14	GND

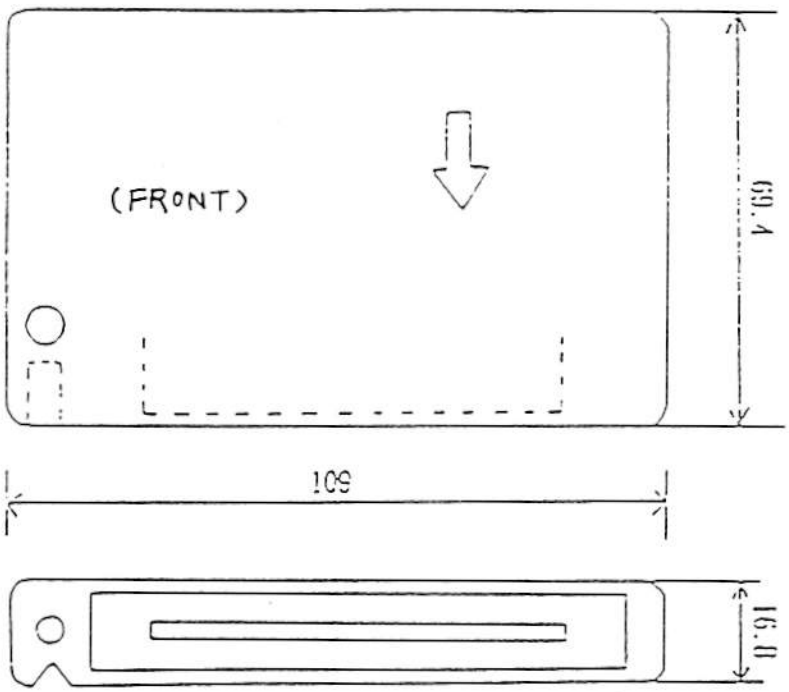
PIN CONNECTION



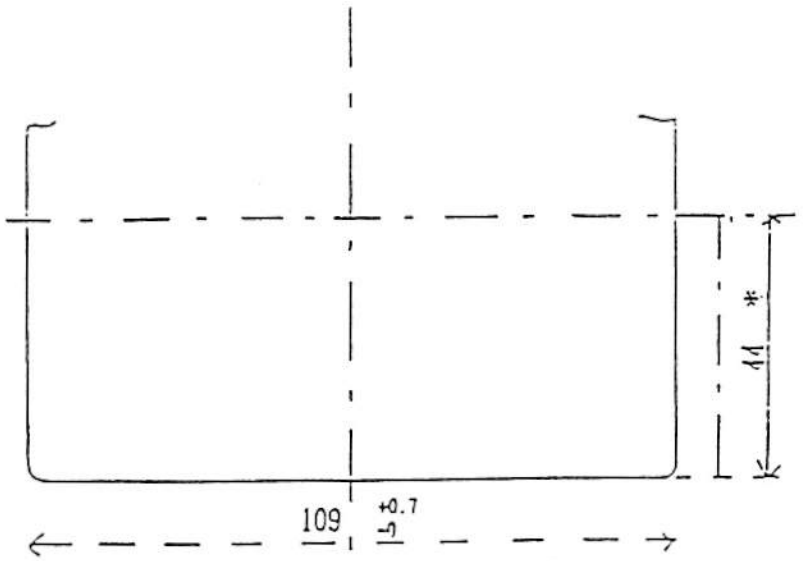
2.5 CARTRIDGE SLOT

2.5.1 SPECIFICATION OF CARTRIDGE

- Physical dimension of the standard cartridge



- Physical dimension of the expanded cartridge



Note: (#) The dimension beyond this size is not specified.

2.5.2 CARTRIDGE

- LIST OF SIGNAL PINS

PIN NO.	NAME	I/O*	PIN NO.	NAME	I/O
1	$\overline{CS1}$	O	2	$\overline{CS2}$	O
3	CS12	O	4	$\overline{SLTSL}$	O
5	RESERVED #	-	6	$\overline{RESH}$	O
7	$\overline{WAIT}$ %	I	8	$\overline{INT}$ %	I
9	$\overline{M1}$	O	10	$\overline{BUSDIR}$	I
11	$\overline{IORQ}$	O	12	$\overline{MERQ}$	O
13	$\overline{WR}$	O	14	$\overline{RD}$	O
15	$\overline{RESET}$	O	16	RESERVED #	-
17	A9	O	18	A15	O
19	A11	O	20	A10	O
21	A7	O	22	A6	O
23	A12	O	24	A8	O
25	A14	O	26	A13	O
27	A1	O	28	A0	O
29	A3	O	30	A2	O
31	A5	O	32	A4	O
33	D1	I/O	34	D0	I/O
35	D3	I/O	36	D2	I/O
37	D5	I/O	38	D4	I/O
39	D7	I/O	40	D6	I/O
41	GND	-	42	CLOCK	O
43	GND	-	44	SW1	-
45	+5V	-	46	SW2	-
47	+5V	-	48	+12V	-
49	SOUNDIN	I	50	-12V	-

* The direction of input/output is based on basic unit side.

Reserved PIN must not be used.

% OPEN COLLECTOR output

- SIGNAL PIN ILLUSTRATION

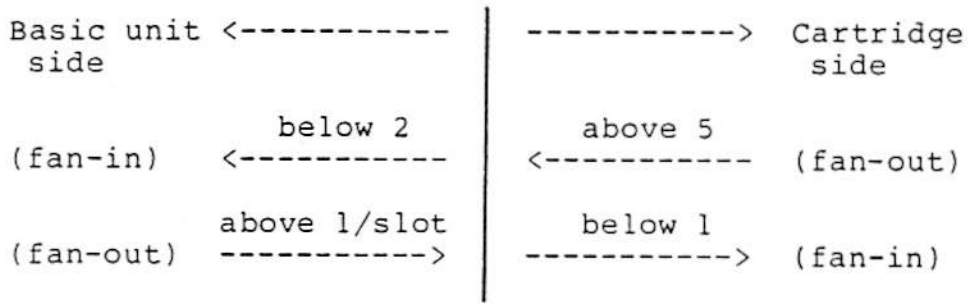
PIN NO.	NAME	DESCRIPTION
1	$\overline{CS1}$ %	ROM 4000-7FFF selected signal
2	$\overline{CS2}$ %	ROM 8000-BFFF selected signal
3	$\overline{CS12}$ %	ROM 4000-BFFF selected signal (for 256K Bit ROM)
4	$\overline{SLTSL}$	Slot select signal
5	RESERVED	For future use only. Do not use this pin.
6	$\overline{RFSH}$	Refresh signal
7	$\overline{WAIT}$	Wait signal to CPU
8	$\overline{INT}$	Interrupt request signal
9	$\overline{M1}$	Fetch cycle signal of CPU
10	$\overline{BUSDIR}$	This signal controlled the direction of external data bus buffer when the cartridge is selected. It is low level when the data is sent by the cartridge.
11	$\overline{IORQ}$	I/O request signal
12	$\overline{MERQ}$	Memory request signal
13	$\overline{WR}$	Write signal
14	$\overline{RD}$	Read signal
15	$\overline{RESET}$	System reset signal
16	RESERVED	For future use only. Do not use this pin.
17-32	A0-A15	Address bus
33-40	D0-D7	Data bus
41	GND	Ground
42	CLOCK	CPU clock 3.579MHz
43	GND	Ground
44, 46	SW1, SW2	Insert/remove detect for protection
45, 47	+5V	+5V power supply
48	+12V	+12V power supply
49	SOUNDIN	Sound input (-5dBm)
50	-12V	-12V power supply

% Note that CS signals imply memory request and read signal

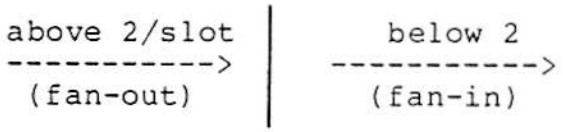
2.5.3 CONDITIONAL OF CARTRIDGE CONNECTION

- Fan-in, fan-out (LS-TTL load)

  Data and Address bus



- Control signals



- Voltage level TTL level

2.5.4 POWER CAPACITY

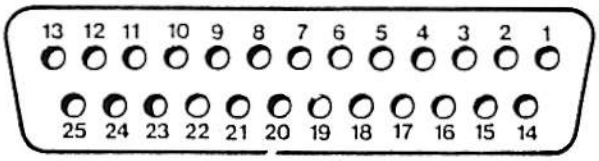
+5V	300mA/Slot
+12V	50mA
-12V	50mA

2.6 SOUND

- LSI	AY-3-8910 compatible
- OCTAVE	8 octave (3 voices output)
- SOUND EFFECT	Yes
- SOFTWARE SOUND OUTPUT	1 bit from output port
- OUTPUT LEVEL	-5dBm (If system has output connector)
- CONNECTOR	RCA 2 pins (If system has audio output connector)

2.7 PIN ASSIGNMENT OF SECOND DRIVE CONNECTOR OF X'PRESS

PIN NO.	SIGNAL NAME	I/O	PIN CONNECTION
1	+12V	-	CONNECTOR PIN LAYOUT: (FEMALE)
2	+5V	-	
3	+5V	-	
4	INDEX	I	
5	DRIVE SELECT 1	O	
6	DIRECTION	O	
7	STEP	O	
8	WRITE DATA	O	
9	WRITE GATE	O	
10	TRACK 0	I	
11	WRITE PROTECT	I	
12	READ DATA	I	
13	SIDE SELECT	O	
14	+12V	-	
15	+12V	-	
16	+5V	-	
17	DRIVE SELECT 0	O	
18	MOTOR ON	O	
19	READY	I	
20-25	GND	-	



2.8 PIN ASSIGNMENT OF THE BUILT-IN 3.5" MICROFLOPPY DRIVE

2.8.1 DC POWER CONNECTOR

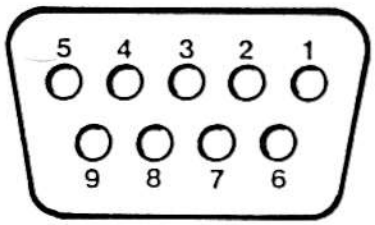
PIN NUMBER	SIGNAL
1	+5 V DC
2	GND
3	GND
4	+12 V DC

2.8.2 INTERFACE SIGNAL CONNECTOR

PIN NO.	SIGNAL	PIN NO.	SIGNAL	I/O
2	(RESERVED)	1	GND	-
4	IN USE	3	GND	I
6	DRIVE SELECT 3	5	GND	-
8	INDEX	7	GND	I
10	DRIVE SELECT 0	9	GND	O
12	DRIVE SELECT 1	11	GND	O
14	DRIVE SELECT 2	13	GND	-
16	MOTOR ON	15	GND	O
18	DIRECTION	17	GND	O
20	STEP	19	GND	O
22	WRITE DATA	21	GND	O
24	WRITE GATE	23	GND	O
26	TRACK 0	25	GND	I
28	WRITE PROTECT	27	GND	I
30	READ DATA	29	GND	I
32	SIDE SELECT	31	GND	O
34	READY	33	GND	I

2.9 PIN ASSIGNMENT OF SVI-738 RS-232C (9-PIN) CONNECTOR

PIN NO.	SIGNAL NAME	I/O	PIN CONNECTION
1	FRAME GROUND	-	CONNECTOR PIN LAYOUT: (FEMALE)
2	TRANSMIT DATA	O	
3	RECEIVE DATA	I	
4	REQUEST TO SEND	O	
5	CLEAR TO SEND	I	
6	DATA SET READY	I	
7	SIGNAL GROUND	-	
8	CARRIER DETECT	I	
9	DATA TERMINAL READY	O	



2.10 KEYBOARD

- LAYOUT : Alphanumerical: ASCII standard
- SCANNING : Software scanning
- NUMBER OF KEYS : 72
- MATRIX DIAGRAM :

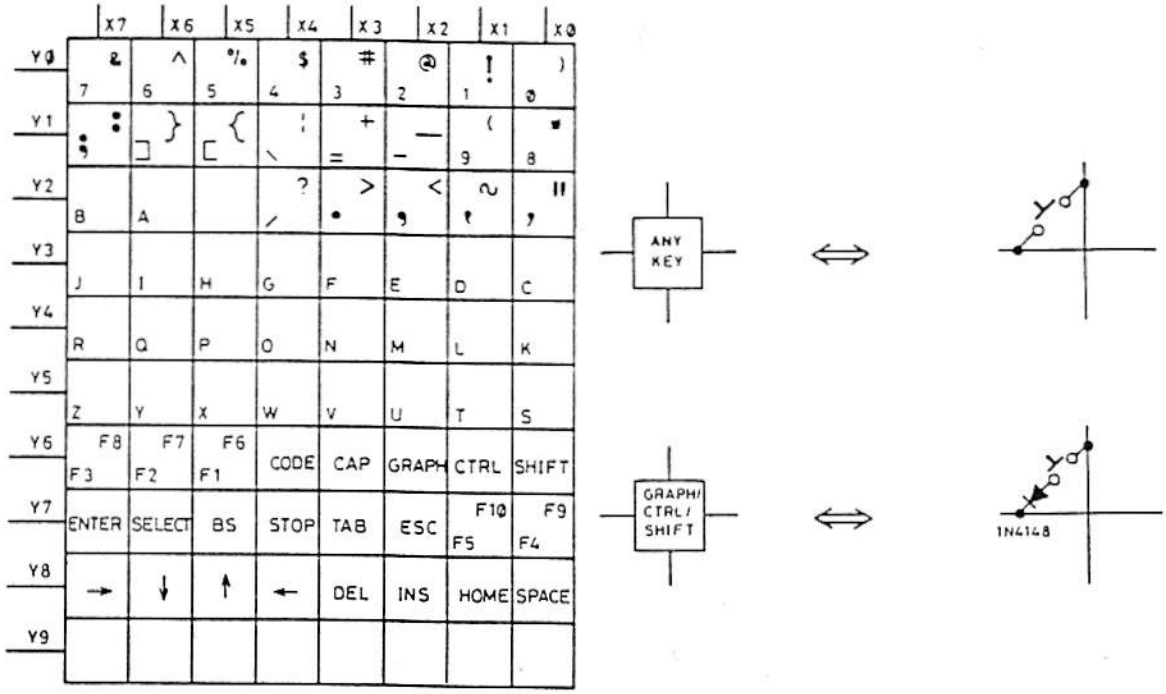
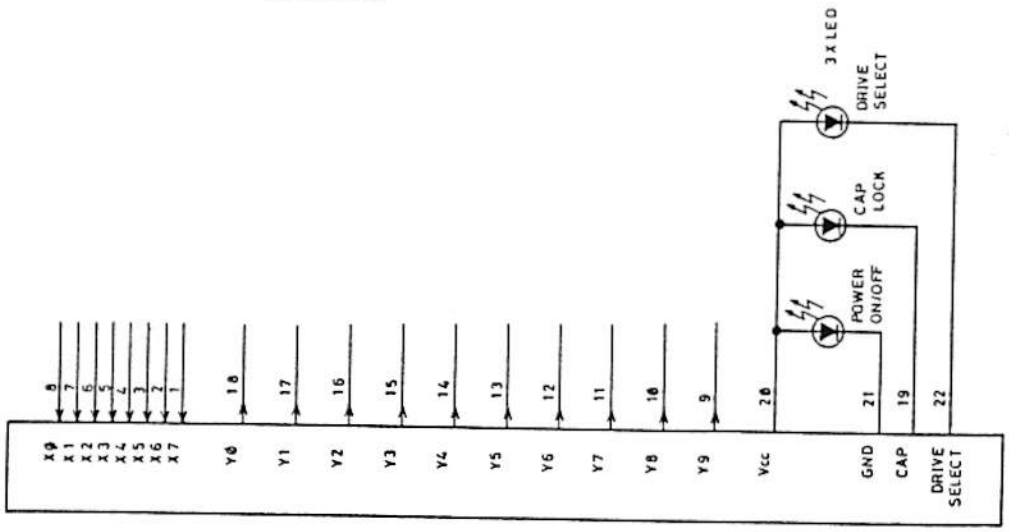
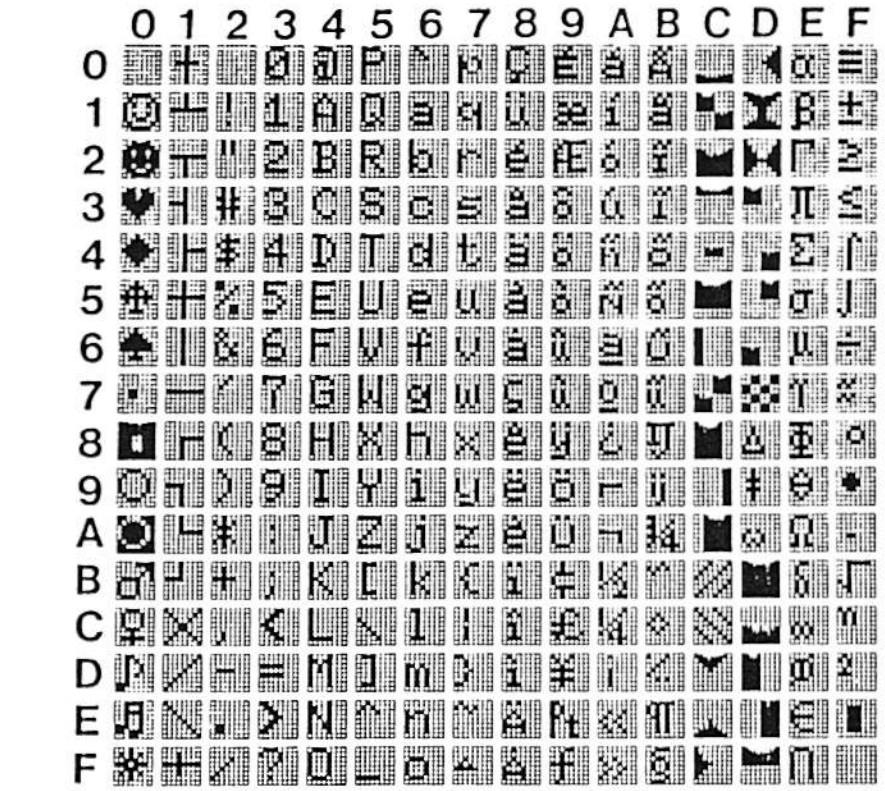


Figure 2.1 X'PRESS international version keyboard matrix



2.10.1 CHARACTER SET FOR MSX



NOTE: The font of the character '0' (zero) is different in DIN version.

Figure 2.2 MSX Character Set

2.10.2 CHARACTER SET FOR CP/M

Figure 2.3 CP/M Character Set

2.10.3 KEYBOARD LAYOUT FOR INTERNATION (INT) AND GERMANY (DIN) VERSION

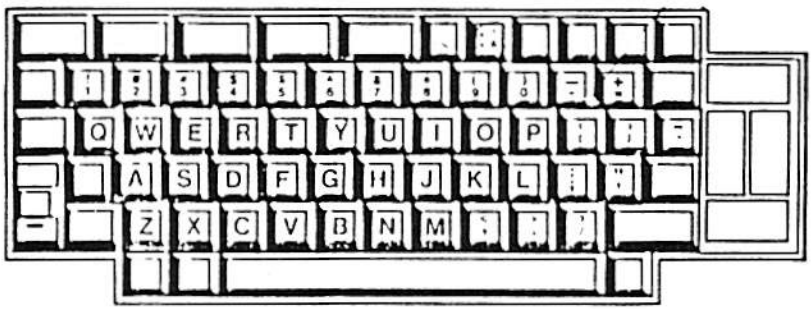


Figure 2.4 Alphanumeric Keys Layout for U.S.A. & INT. Version

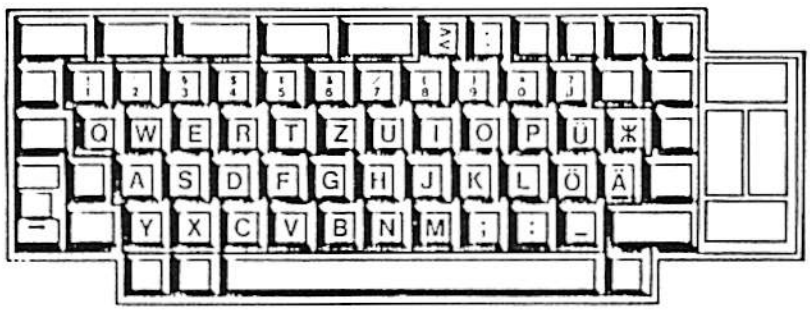


Figure 2.5 The alphanumeric Keys Layout for DIN Version

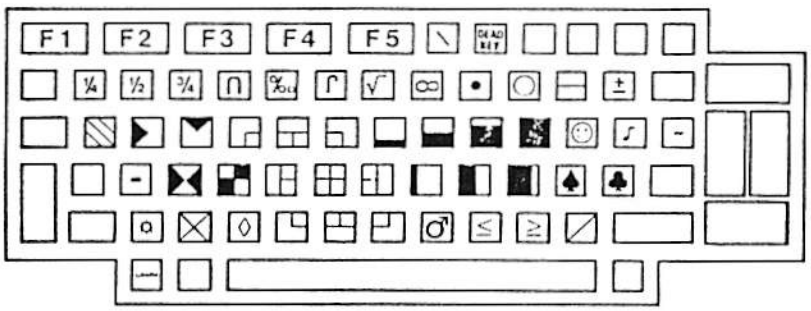


Figure 2.6 Keyboard with Graph Key Pressed (U.S.A. & INT. Version)

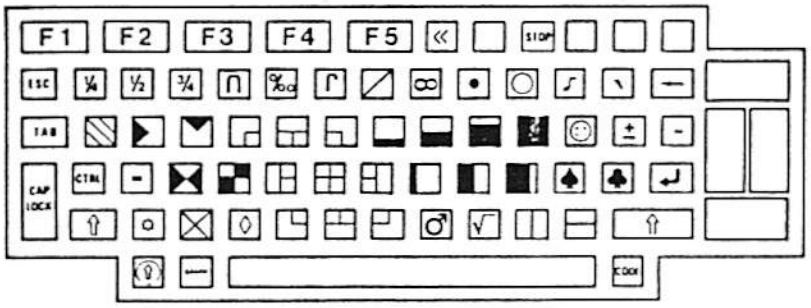


Figure 2.7 Keyboard with Graph Keys Pressed (DIN Version)

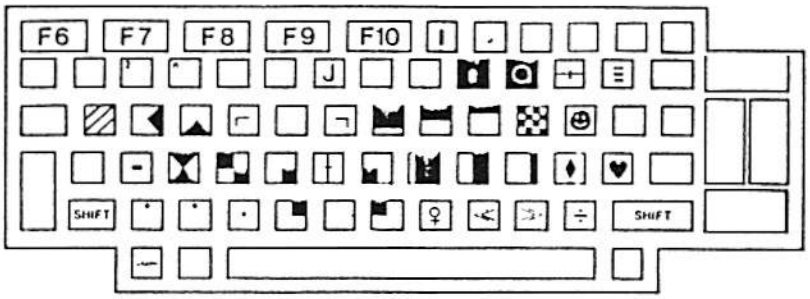


Figure 2.8 Keyboard with Shift & Graph Keys Pressed (U.S.A. & INT. Version)

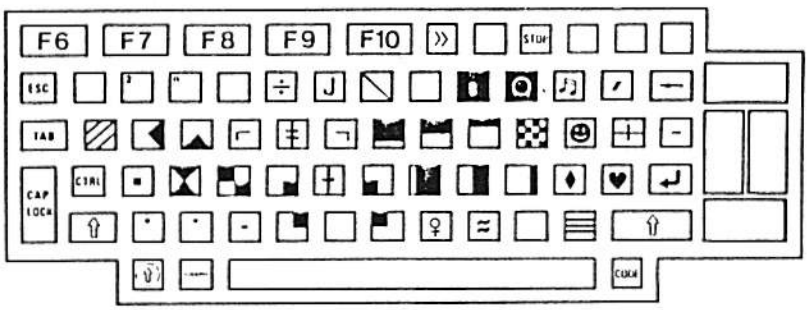


Figure 2.9 Keyboard with Graph & Shift Keys Pressed (DIN Version)

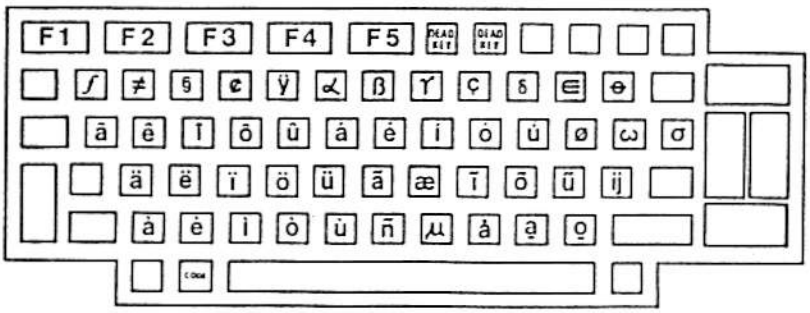


Figure 2.10 Keyboard with Code Key Pressed (U.S.A. & INT. Version)

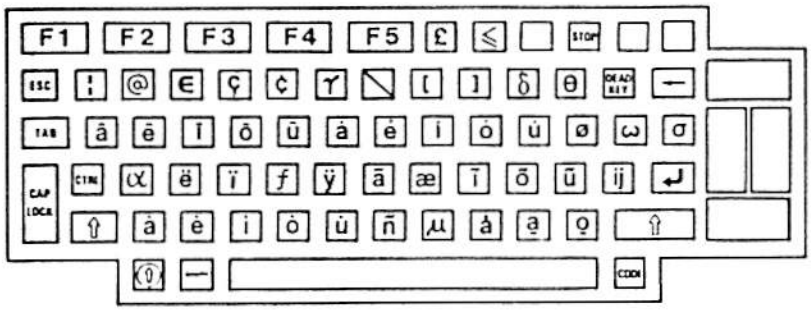


Figure 2.11 Keyboard with Code Key Pressed (DIN Version)

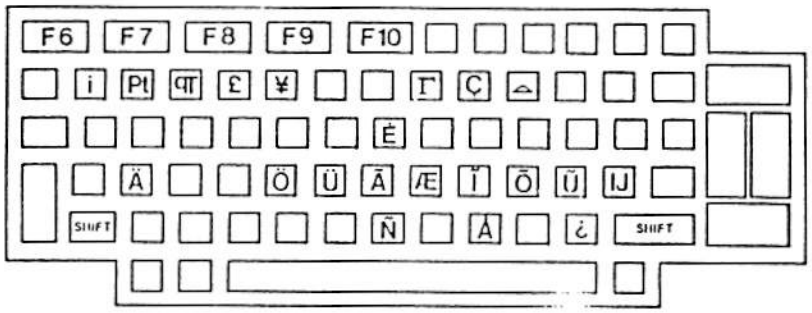


Figure 2.12 Keyboard with Shift & Code Keys Pressed (U.S.A. & INT. Version)

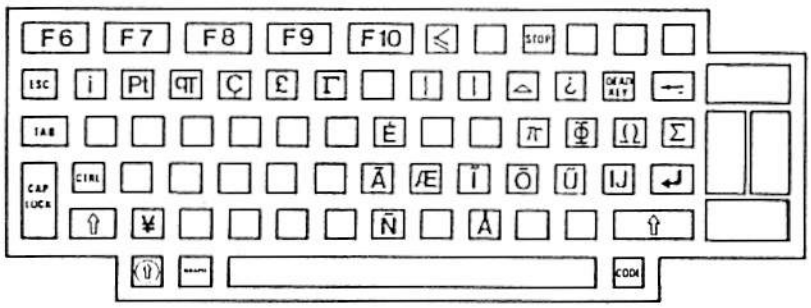


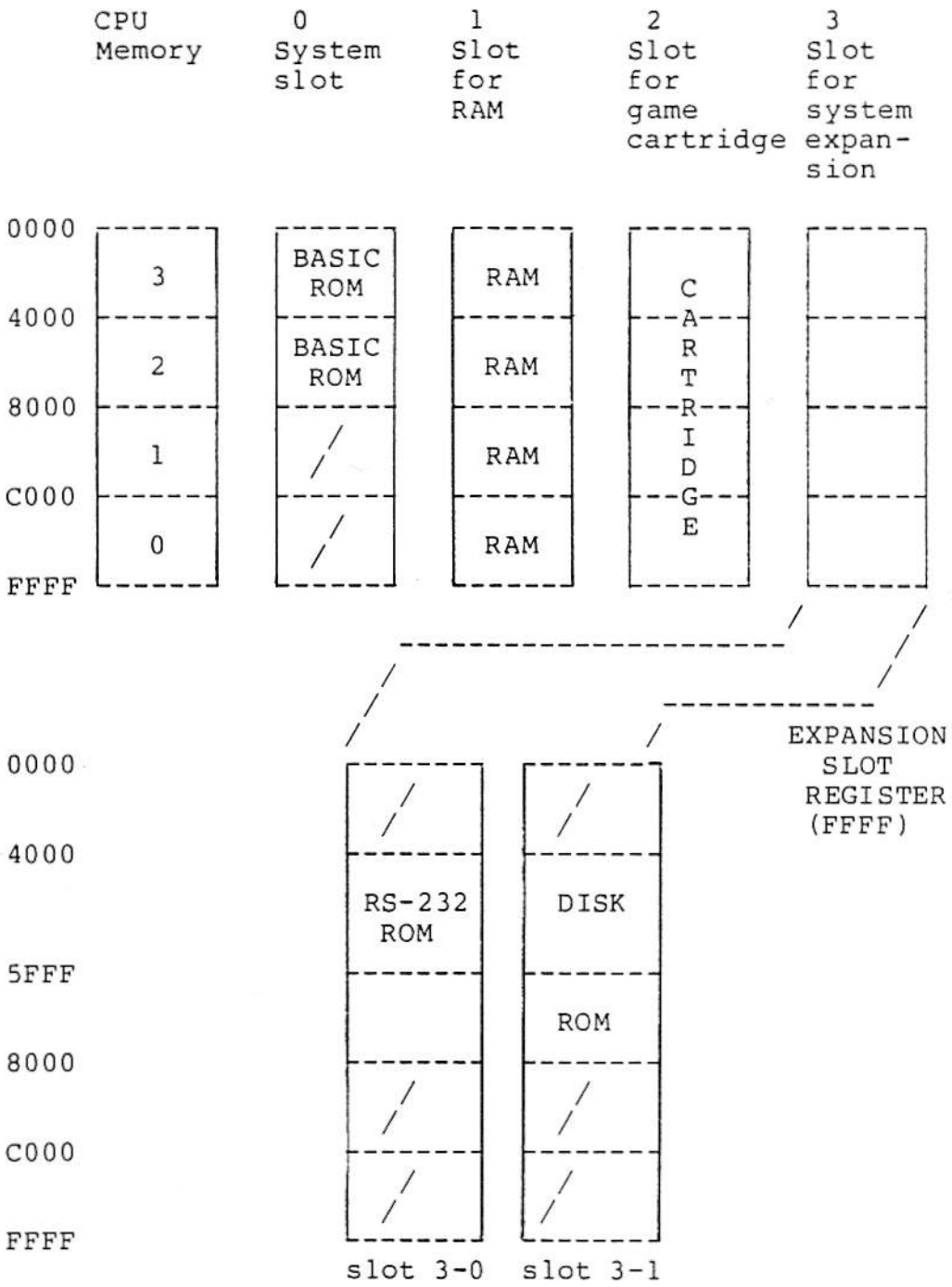
Figure 2.13 Keyboard with Shift & Code Keys Pressed (DIN Version)

CHAPTER 3

MEMORY SYSTEM

3.1 MEMORY MAP

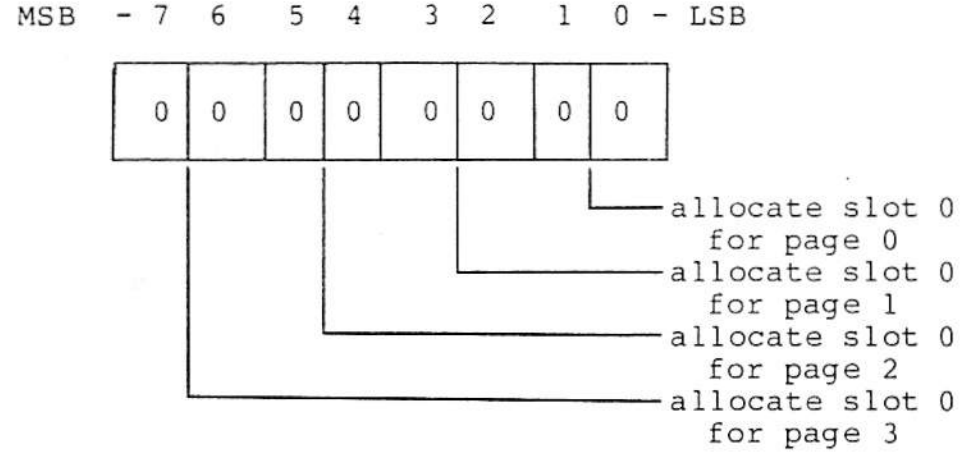
- Following is the memory map for SVI-738 computer.



- MSX BASIC uses the largest available RAM area that is installed from FFFF to 8000 contagious for its system working RAM area. This can be placed on any slots including expanded slots.

- Basic (primary) slot select register, which is the port A of 8255, maps physical memory space to the logical CPU memory space in 16K bytes unit (page).

  For example, following value in slot select register allocates page 0 and 1 from slot 0, page 2 from slot 2 and page 3 from slot 0.



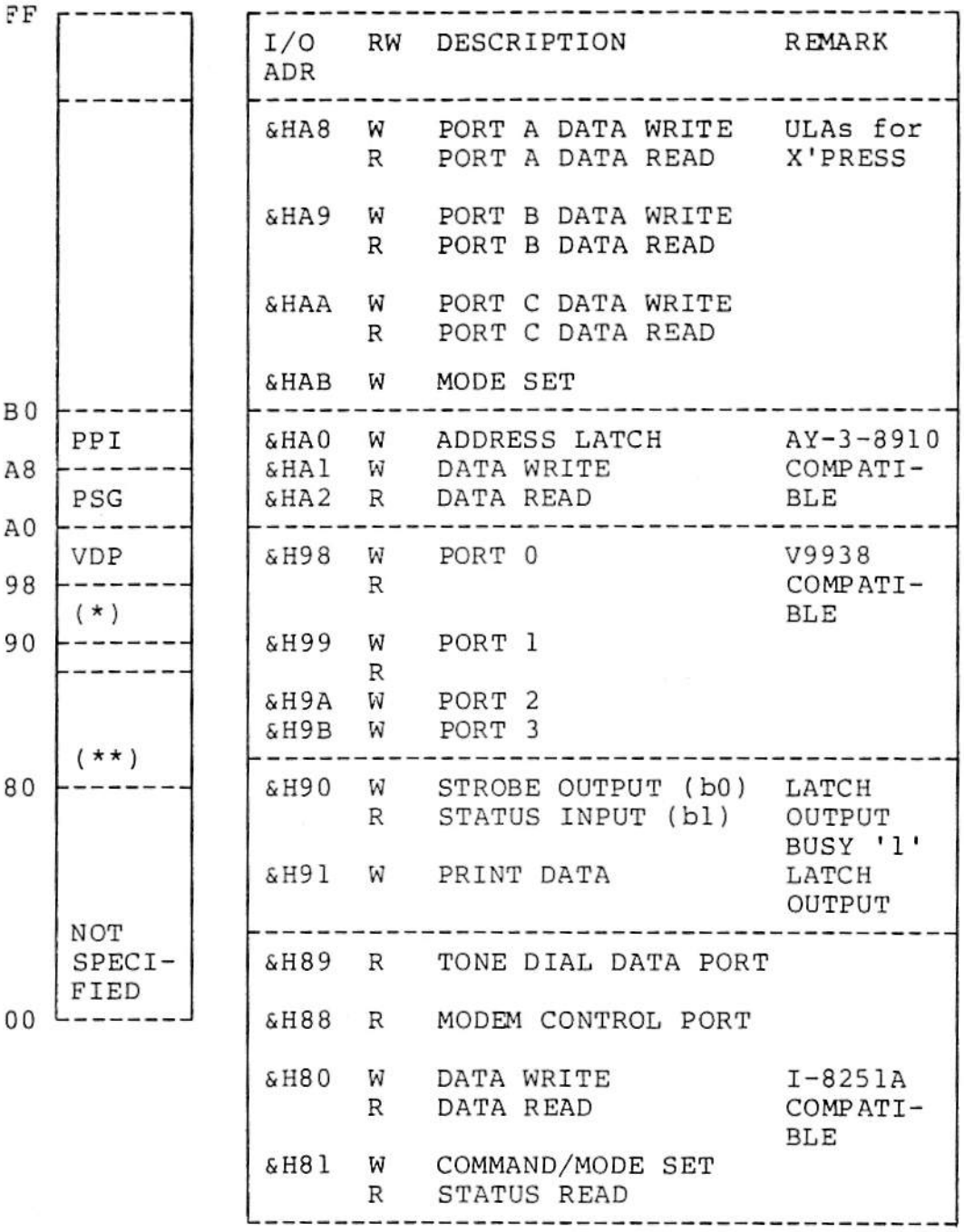
- Slot 3 is expanded to give two more system slots via Expansion (secondary) slot select register. The location of slot select register for the expanded slots is memory address FFFF of the primary slot. And to make it possible to differentiate the register from the ordinary RAM, complement the output of the register. That is, when read the register, the read data is the complement of the actual value of the register.

  The physical memory is always allocated to same memory page in the CPU address space. It is not possible to allocate to different page like page 3 of slot 3 to page 0 of CPU memory space.

Notes: The meaning of "slot" does not imply that is must has connector for cartridge, however, the slot for cartridge must have connector, of course. Refer to APPENDIX B I/O INTERFACE.

I/O MAP

I/O ADDRESS DEVICE



I/O ADR	RW	DESCRIPTION	REMARK
&HA8	W	PORT A DATA WRITE	ULAs for
	R	PORT A DATA READ	X'PRESS
&HA9	W	PORT B DATA WRITE	
	R	PORT B DATA READ	
&HAA	W	PORT C DATA WRITE	
	R	PORT C DATA READ	
&HAB	W	MODE SET	
&HA0	W	ADDRESS LATCH	AY-3-8910
&HA1	W	DATA WRITE	COMPATI-
&HA2	R	DATA READ	BLE
&H98	W	PORT 0	V9938
	R		COMPATI-
			BLE
&H99	W	PORT 1	
	R		
&H9A	W	PORT 2	
&H9B	W	PORT 3	
&H90	W	STROBE OUTPUT (b0)	LATCH
	R	STATUS INPUT (b1)	OUTPUT
			BUSY '1'
&H91	W	PRINT DATA	LATCH
			OUTPUT
&H89	R	TONE DIAL DATA PORT	
&H88	R	MODEM CONTROL PORT	
&H80	W	DATA WRITE	I-8251A
	R	DATA READ	COMPATI-
			BLE
&H81	W	COMMAND/MODE SET	
	R	STATUS READ	

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3.4 PSG BIT ASSIGNMENT

PORT	BIT	I/O	CONNECTOR PIN NO.	SIGNALS FOR JOYSTICK
A	0		J3-1 PIN	
			J4-1 PIN* #2	FWD2
	1		J3-2 PIN #1	BACK1
			J4-2 PIN* #2	BACK2
	2		J3-3 PIN #1	LEFT1
			J4-3 PIN* #2	LEFT2
	3		J3-4 PIN #1	RIGHT1
			J4-4 PIN* #2	RIGHT2
	4		J3-6 PIN #1	TRGA1
			J4-6 PIN* #2	TRGA2
	5		J3-7 PIN #1	TRGB1
			J4-7 PIN* #2	TRGB2
	6			
	7		CSAR (CASSETTE TAPE READ)	
B	0		J3-6 PIN #3	
	1		J3-7 PIN #3	"H" LEVEL
	2		J4-6 PIN* #3	
	3		J4-7 PIN* #3	
	4		J3-8 PIN	
	5		J4-8 PIN*	
	6		PORT A (INPUT SELECT)	
	7			

#1 Available when bit 6 of port B is low used by JOYSTICK 1

#2 Available when bit 6 of port B is high used by JOYSTICK 2

#3 Make the "H" level, when used as an output port. Tied an open collector buffer to the output (Refer to APPENDIX C-1)

Remark PIN5 +5V
PIN9 GND

- On the minimum system, signals are not connected to J4

3.5 I/O MAPPING OF BUILT-IN MICROFLOPPY DRIVE

SLOT	I/O ADDRESS	R/W	DESCRIPTION
3-1	7FB8	W	Command port of 1793
	7FB8	R	Status port of 1793
	7FB9	R/W	Track register of 1793
	7FBA	R/W	Sector register of 1793
	7FBB	R/W	Data register of 1793
	7FBC	R	(MSB) Bit 7 - interrupt of 1793 (1 for interrupt)
			Bit 6 - data request of 1793 (0 for request)
	7FBC	W	Bit 3 - motor on (1 for ON)
			Bit 2 - side select (0 for side 0)
			(LSB) Bit 0 - drive enable (1 for ENABLE)

CHAPTER 4

SVI-738 X'PRESS' PERIPHERALS

4.1 SVI-767 MSX DATA CASSETTE

The SVI-767 is an inexpensive device that uses ordinary cassette tape to add storage and retrieval capability to the computer system. The built-in Automatic Level Control (ALC) ensures reliable and high quality recording. Tape Counter, LED indicator and auto-stop are standard features.

SPECIFICATION

Power	:	12V DC
Current Consumption		
• Motor off	:	20mA ± 5mA
• Motor on	:	140mA ± 10mA
Plan Gain		
• 1 KHz (-90db in)	:	0.95V ± 0.2V (board level at power amp. input)
• 6 KHz (-90db in)	:	0.85V ± 0.2V
• 1 KHz	:	2.3V ± 0.5V (at data output)
• 6 KHz	:	2.0V ± 0.5V
Play Level	:	3.5V ± 0.2V p-p
DC Noise	:	<80mV
Erase Noise	:	<230mV

4.2 SVI-777 MSX STRINGY FLOPPY DRIVE

Employing an advanced tape drive, the Stringy Floppy Drive adds up to 100K of long-term storage. This inexpensive device, controlled by its own operating system, stores files on rugged, compact cartridges, called Microwafer™. Fast, accurate, file storage and retrieval are a snap with the Stringy Floppy.

SPECIFICATION

External Dimension : 63 x 153 x 198 (H x W x D mm)

Features

- Front : - Insert Slot
  - "In Use" and "Power" Indicatiors
- Rear : - Power Switch
  - External Cassette Socket
  - Cassette and Joystick Plugs for connection

Power Source : - 2 size D (VM-1) 1.5V batteries for motor (batteries life approximately 6 hrs/day a month)
- 5V Power Supply for system for console directly

Data Transfer Rate : 13.2 Kbit/sec
(11 times faster than data cassette)

Tape Capacity (approximately) :

Length (ft)	Capacity (Kbytes)
10	14
20	26
35	52
50	74
62	100

Microwafer is a trademark of Entrepo, Incorporated

4.3 SVI-787 MICROFLOPPY DISK DRIVE

Matching the X'PRESS in colour, design and performance, SVI-787 is the perfect compliment to your computer system. This 3.5" disk drive doubles the long-term storage capacity of your computer. With the built-in disk drive controller in the X'PRESS, this unit can hook up directly to the X'PRESS. And it works with all three popular microcomputer operating systems: MSX-DOS, CP/M and MSX DISK BASIC.

SPECIFICATION

Drive Unit	:	Single
Floppy Diskette	:	- Single sided - Double track - Soft sectored 3.5" diskette
Memory Capacity		
• Unformatted	:	500K bytes
• Formatted	:	328K bytes
Disk Operating System	:	- MSX DOS - CP/M DOS - MSX DISK BASIC
Rotational Speed	:	300 rpm
Disk Format	:	CP/M - 80 tracks 1 side - 17 sectors / track - 256 bytes / sector MSX DOS - 80 tracks 1 side - 9 sectors / track - 512 bytes / sector
Access Time	:	- Seek time 6/3 msec - Setting time 15 msec - Motor start time 400 msec - Average access time 173/94 msec
Recording Density	:	8187 BPI
Track Density	:	135 TPI
Encoding Method	:	MFM
Power Source	:	Supplied from Console

Relative Humidity

- Operating : 20 to 80% (non-condensing)
- Transportation and Storage : 8 to 90% (non-condensing)

Ambient Temperature

- Operating : 5 to 50°C
  Max. temperature deviation - 10°C/H
  (10 to 60°C for disk)

4.4 SVI-709 MSX NETWORK INTERFACE CARD

This cartridge transforms your computer into a station in the SVI-609 Local Area Network. These stations are given access to the mass-storage and rapid printing resources of the SVI-609 Master Station. Each slave station can make use of a portion of the SVI-609's 10M-bytes hard disk for its own file storage, and all stations can share a common storage area, printer spooler and software library.

4.5 SVI-105M MSX GRAPHIC TABLET

The SVI-105M Graphic Tablet is designed to be used with MSX compatible computer with 64K RAM. It enables you to draw in 12 modes and 16 colours. The graphics can be saved on a data cassette tape by using a SVI-767 or any other standard cassette recorder. To print the graphics, you can use a EPSON FX-80 Dot Matrix (or compatible) printer.

With the SVI-105M Graphic Tablet, you can create your masterpiece leisurely on a TV screen with a blunt stylus or even with your finger!

4.6 SVI QUICKSHOT SERIES FOR MSX COMPUTER SYSTEM

4.6.1 SVI-101M QUICKSHOT I

The Quickshot I MSX Joystick has 2 separate fire buttons for the many new games that requires 2 buttons to play. An improvement of the original award-winning "Quickshot" design, the SVI-101 enhances the excitement and arcade flavour of your game play. It's a sure winner!

4.6.2 SVI-102M QUICKSHOT II

The Quickshot II MSX Joystick is the upgraded model of the original Quickshot. It has a locking auto fire switch and dual fire buttons. Top fire button is an extra large, curving back towards rear of joystick to give more comfortable and more fun.

4.6.3 SVI-107M QUICKSHOT VII

The Quickshot VII is designed to help you get the most out of your video games. All eight directions are available at the touch of a finger tip. The touch-sensitive control pad makes it easy to maneuvre your player - even though the most complex maze. while two fire buttons, both with auto-firing capabilities, ensures that your weapons are ready whenever you are. And to monitor their response, one independent LED registers the status of each button.

4.6.4 SVI-109M QUICKSHOT IX

Quickshot IX brings you the most innovative video entertainment product since Pong. The Joyball. A new breed of game controller, a hybrid resulting from the cross between a joystick and a trackball.

Combining the precision of a joystick with the fatique-free operation of a trackball, the Joyball sets a new standard for performance. The reliability is enhanced by the installation of the customised micro switches used and the spherical control.

CHAPTER 5

DISSASSEMBLY/ASSEMBLY

This chapter contains step by step procedure for disassembling and reassembling of SVI-738. Read this chapter over carefully and follow the procedure given before attempting to disassemble the computer.

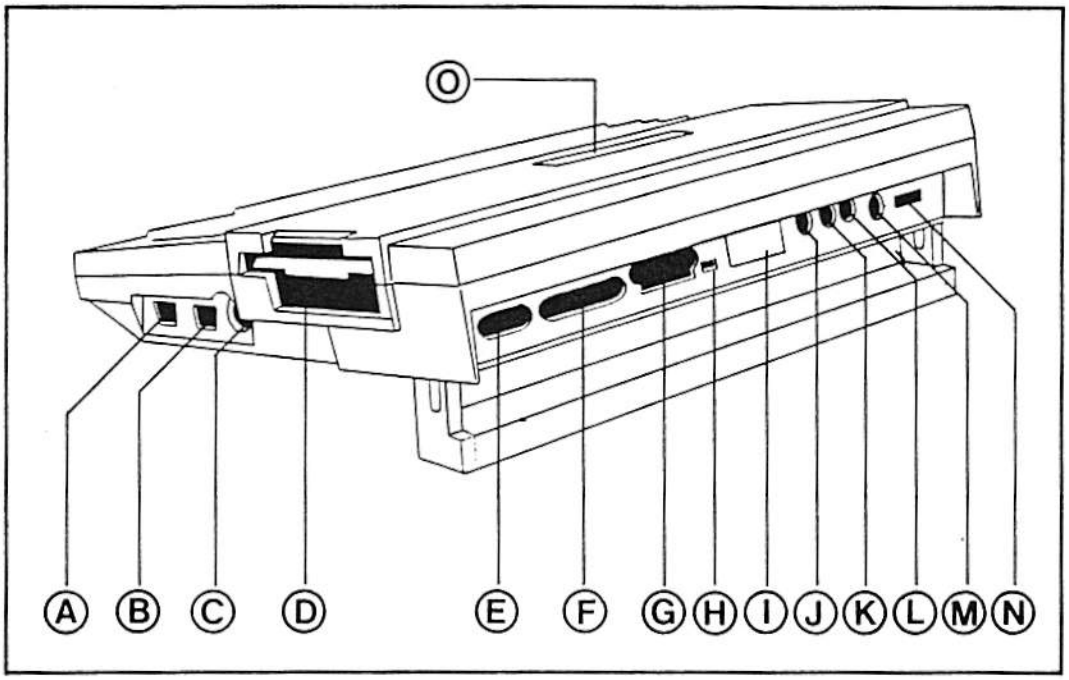


Figure 5.1 Location of I/O Ports of SVI-738

A. Joystick (I/O) Port 1
B. Joystick (I/O) Port 2
C. Cassette (I/O) Port
D. Microfloppy Slot
E. RS-232C Port
F. Second Disk Drive Port
G. Printer Port
H. Channel Switch*
I. Name Tag
J. Modulator Output Port
K. Monitor Video Port
L. Monitor Audio Port
M. Power Socket
N. Power Switch
O. MSX Standard Cartridge Slot

* Available for some countries only.

5.1 GENERAL CAUTION

(1) Be very careful about mixing screws. There are 2 types of screws; self-tap and machine screw. If wrong size or type of screws are used permanment, damage to both the screws and the plastic housing may results.

(2) Never tighten the screws too tight, this will stripe the plastic housings for the self-tap screws.

(3) Be very careful with the Flex Cable; never fold them.

(4) Use soft-padding when turning the Console bottom up, in order to prevent damange to the plastic surfaces.

(5) Static control precautions must be used when handling any Printed Circuit Board.

(6) Never switch on the power when the Heat Sink Plate is removed, this will cause damage to IC1 and to IC2 in Power Board.

(7) Make sure that the computer is free from all external cables before starting the disassembling procedure.

5.2 KEYBOARD AND PCB ACCESS

(1) Turn the Console bottom up.

(2) Loosen and remove 6 self-tap screws from the Bottom Housing (See figure 5.2).

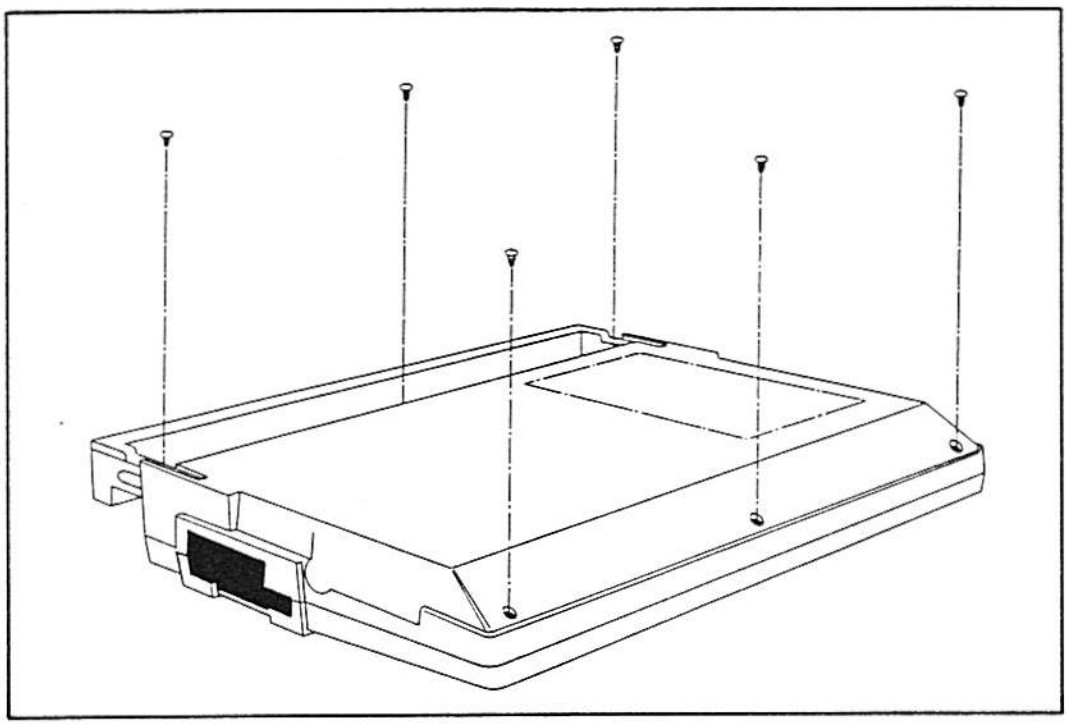


Figure 5.2 Location of Screws on Bottom Housing

(3) Turn the Console up right again.

(4) With the front of the Console facing you, carefully lift up the Keyboard and flip it over towards you. (See figure 5.3)

(5) In some countries, a metal shielding cover is required. It can be removed by loosening the self-tap screws found on it.

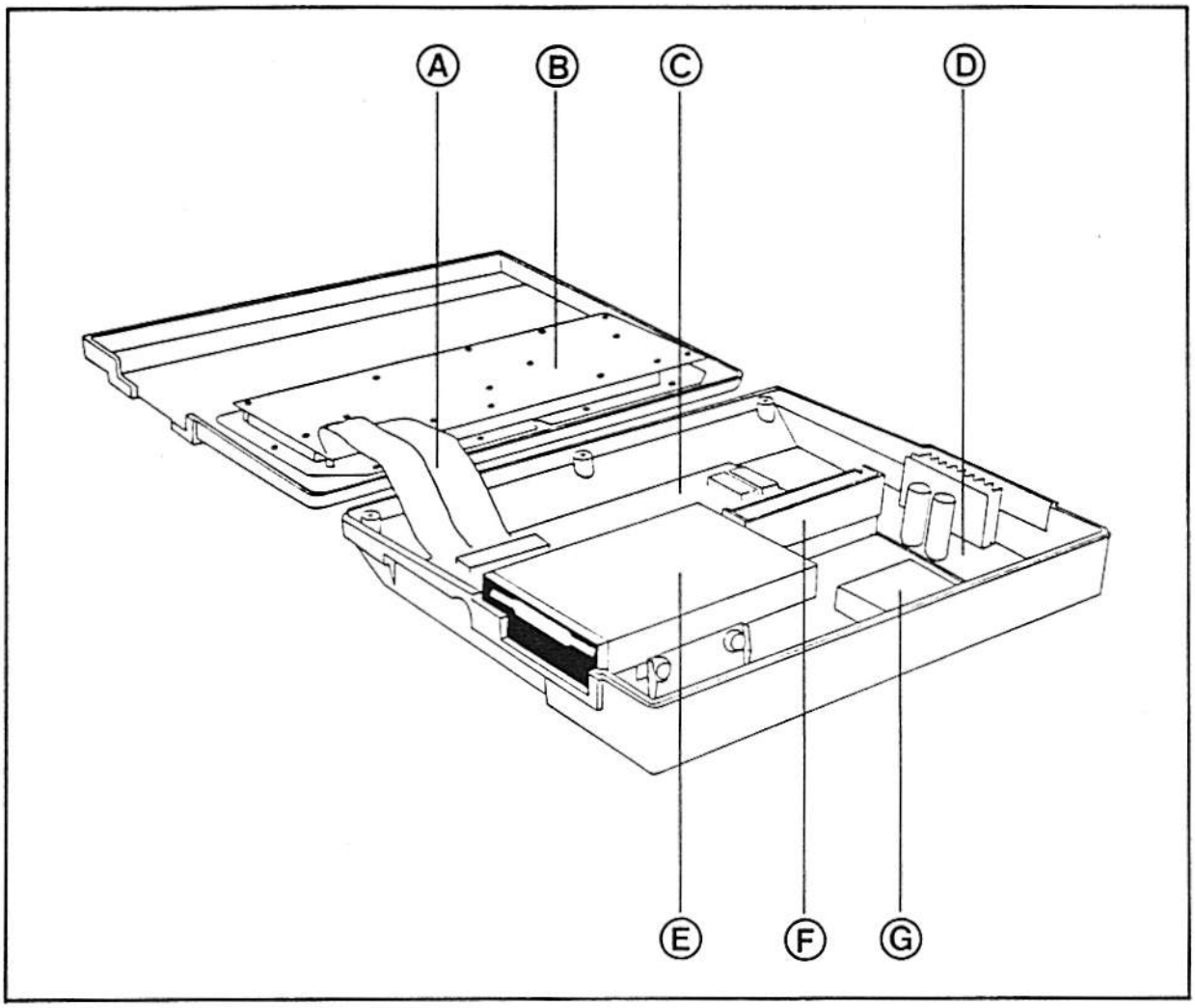


Figure 5.3 Internal Components of SVI-738

A. Flex Cable
B. Keyboard PCB
C. Main Logic Board
D. Power Board
E. Microfloppy Drive
F. Cartridge Support
G. Modulator

5.3 REASSEMBLE OF THE CONSOLE

(1) Carefully flip the Keyboard up right so that is is on top of the Bottom Housing.

(2) Gently (do not force) lower the Keyboard onto the Bottom Housing, until the 2 snap in place together.

(3) Turn the Console up side down.

(4) Tighten the 6 self-tap screws. (See figure 5.2)

(5) Turn the unit right side up again when done.

5.4 REMOVAL OF THE BUILT-IN MICROFLOPPY DRIVE AND CARTRIDGE SUPPORT

(1) Loosen the 4 machine screws attached to the Microfloppy and Main Logic Board. (See figure 5.4)

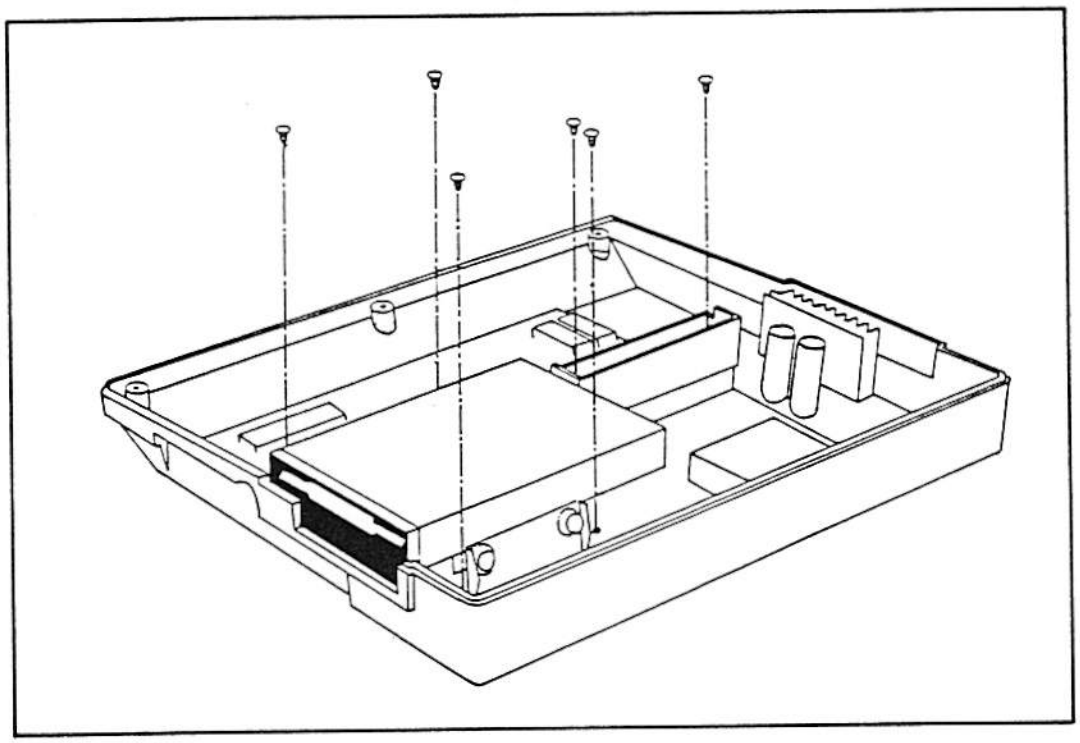


Figure 5.4 Location of Screws on the Microfloppy and Cartridge Support

(2) Gently disconnect the interface and power cables of the microfloppy drive.

(3) Remove the microfloppy drive and put it in a safe place.

(4) Unscrew the 2 machine screws in the cartridge slot. (See figure 5.4)

(5) Remove the cartridge support and the whole picture of the Main Logic Board will be seen.

5.5 REINSTALLING OF THE MICROFLOPPY DRIVE AND CARTRIDGE SUPPORT

Basically, it is a reverse of procedures listed in section 5.4 but there is a few things which needs attention.

(1) The interface and power cables of the microfloppy must be folded outward so that it does not interfere with the drive operation.

(2) Watch out for the polarity mark in the cable connector.

5.6 REMOVAL OF POWER BOARD

(1) Loosen the 3 machine screws on the power board. (See figure 5.5)

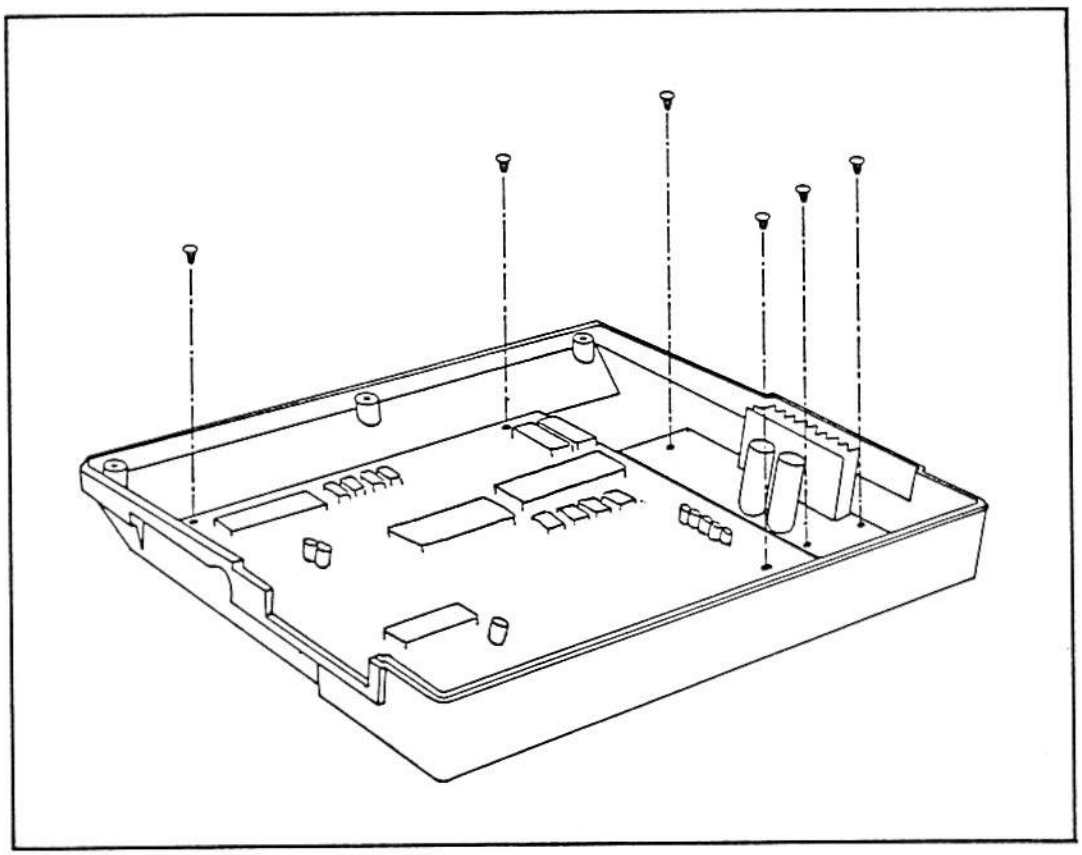


Figure 5.5 Location of Screws on the Printed Circuit Board

(2) Slide the whole-board towards the keyboard and gently lift it up.

(3) Rotate the unit 90 degrees until it is perpendicular to the bottom housing and insert the edge of the unit into one of the ventilation openings when doing trouble shooting with the Power Board. (See figure 5.6)

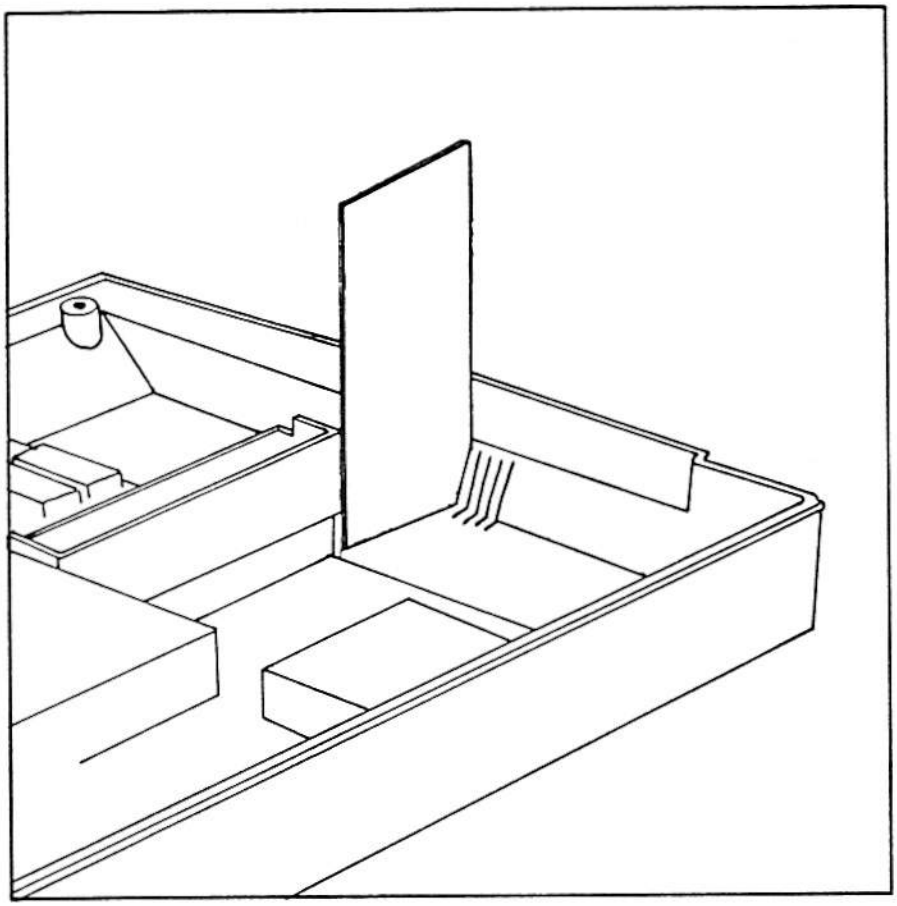


Figure 5.6 Position of the Power Board for Easy Access to the Components

5.7 REINSTALLING THE POWER BOARD

Reverse the procedures listed in section 5.6.

5.8 REMOVAL OF THE MAIN LOGIC BOARD

Caution: Since the Main Logic Board and the Power Board are linked together by power cables, it is advised to remove the two as one unit in order to minimize possible damage.

(1) Loosen the 3 machine screws on the Main Logic Board. (See figure 5.5)

(2) Gently slide the Logic Board towards power unit until the 2 joystick and cassette ports are inside the housing.

(3) Lift up the Logic Board and slide it towards the keyboard until the socket clamps of the printer port are inside the housing.

(4) Gently remove the whole unit from the bottom housing.

5.9 REINSTALLATION OF MAIN LOGIC BOARD

(1) Insert the Power Switch and Power Socket into their respective slots.

(2) Insert the clamps for the Printer Cable into the Printer Slot.

(3) Slide the Joystick Ports into their respective slots.

(4) Tighten the screw.

5.10 REMOVAL OF KEYBOARD ASSEMBLY FROM UPPER HOUSING

Note: When disassembling the Keyboard be very careful with the Flex Cable.

(1) Carefully flip the Top Housing of the Console up side down. (See figure 5.4)

(2) Locate and loosen 10 self-tap screws. (See figure 5.7)

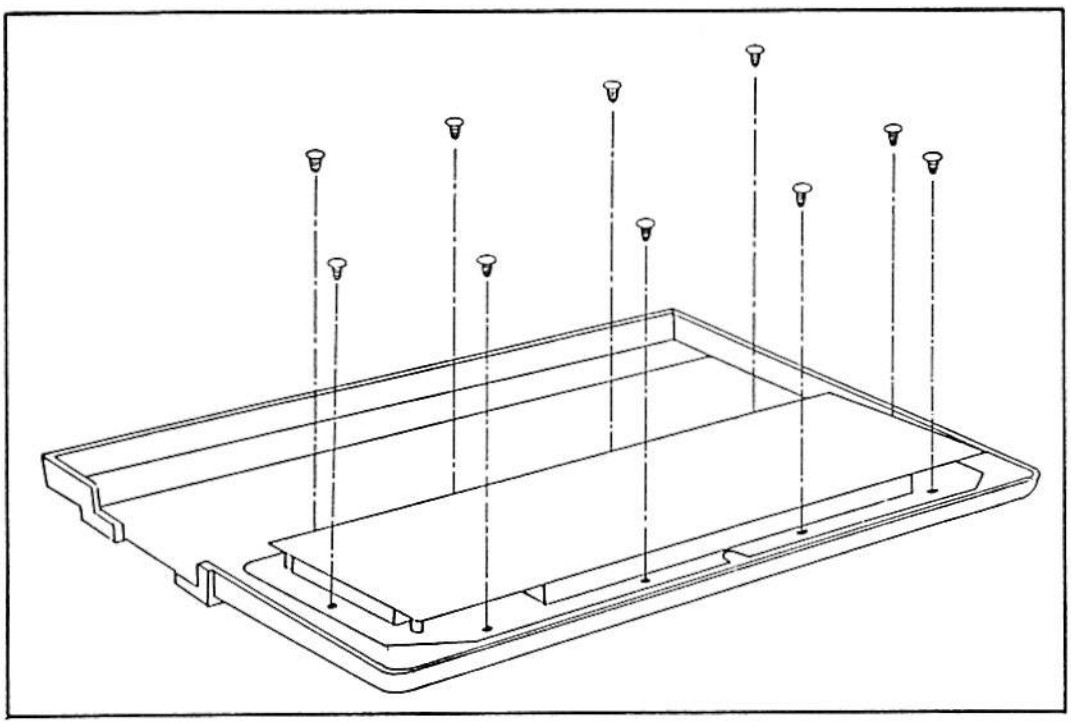


Figure 5.7 Location of the Screws on the Uppwer Housing

(3) The Keyboard Assembly can now be removed from the Top Housing.

5.11 REINSTALLATION OF KEYBOARD ASSEMBLY TO UPPER HOUSING

To reinstall, reverse the procedure listed in section 5.10.

5.12 REMOVAL OF KEYTOPS

(1) Figure 5.8 shows the cross section of a single Keytop.

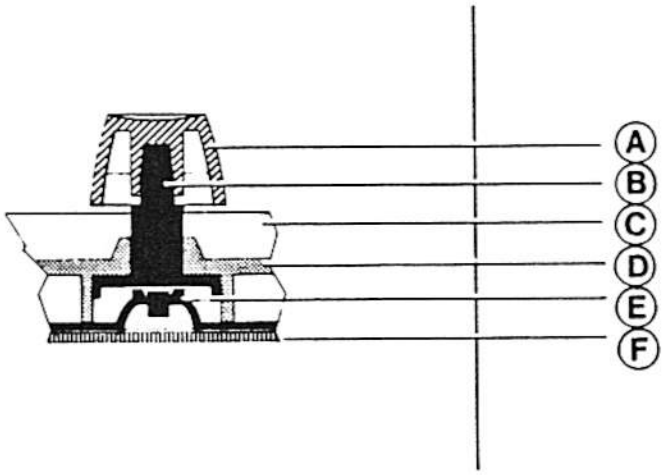


Figure 5.8 Cross Section of a Single Keytop

A. Keytop	D. Template
B. Key Shaft	E. Rubber Spacer
C. Upper Casing	F. PCB

(2) Use a flat head screw driver to gently (do not force) ply off the Keytop except for the Space Bar.

(3) To remove the Space Bar, gently ply at the middle of it until it is free from the Key Shaft.

(4) Free the Hing Rod from the Hing Rod Holders.

(5) Now the Space Bar can be removed. Be careful not to lose the Spring which is attached to the Key Shaft.

5.13 REINSTALLATION OF KEYTOPS

(1) To install the Space Bar, position the Sping so that it is inside the Spring Holder.

(2) Snap the Hing Rod into the Hing Rod Holders.

(3) Push the Key Shaft down, and place the Space Bar over the Key Shaft.

(4) Check and make sure that the latches (which are white in colour) fall properly into their openings. If it does not, then free the Hing Rod from the Hing Rod Holders and turned the Spacer Bar around and repeat the above procedures.

(5) Align the Key Shaft with the Space Bar and push down at the middle of the Space Bar.

(6) To reinstall the Keytop, align it with the Key Shaft and push down on it.

(7) Repeat the above step until all the Keytops has been reinstalled.

5.14 DISASSEMBLE OF KEYBOARD ASSEMBLY

(1) Figure 5.9 shows the 6 levels of the Keyboard Assembly.

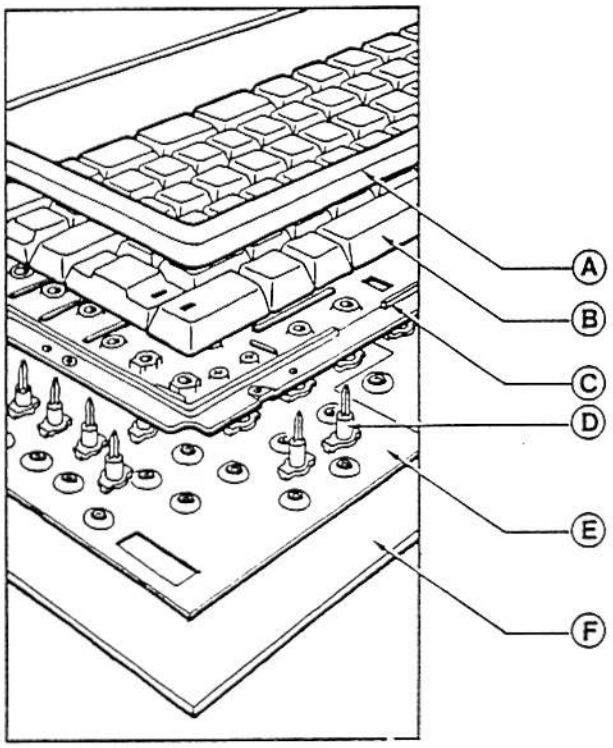


Figure 5.9 6 Levels of the Keyboard Assembly

A. Upper Housing
B. Key Tops
C. Template
D. Key Shaft
E. Rubber Spacer with Silicon Conductor
F. Keyboard PCB

(2) To disassemble, locate the loosen 15 self-tap screws on the Keyboard PCB. (See figure 5.10)

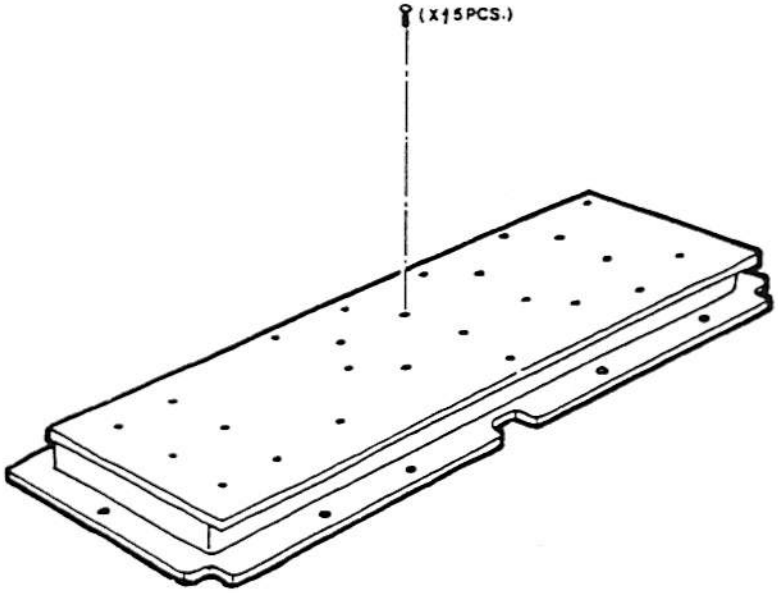


Figure 5.10 Location of Screws on Keyboard PCB

(3) Remove the Keyboard PCB.

(4) Remove the Rubber Spacer.

(5) Turn the unit right side up.

(6) Follow sections 5.12 and 5.13 for removal and reinstallation of Keytops and Space Bar.

5.15 REASSEMBLE OF KEYBOARD ASSEMBLY

Reverse the procedure listed in section 5.14 for reassembling of Keyboard Assembly.

CHAPTER 6

TROUBLE SHOOTING

This chapter is intended to give an average technicians clues in repairing SVI-738 computer system. A quick reference table is given in symptom checklist for fast repairing needs. A detail step-by-step diagnostic flowchart is given in 6.3 for full system check. A test cartridge is needed for diagnosis to perform.

6.1 SWAP OUT PROCEDURE

At many places in the diagnostic flowcharts or symptom checklist, a chip or a number of chips has to "swap-out" in particular order. The "swap-out" instruction means that you should replace the indicated components (one at a time) with a known good component of the same type. The SVI-738 should then be tested with the new, known-good component in place to see whether the "swap-out" solved the problem being checked. If the swap-out did not fix the problem, the known-good component should be removed, and the original component reinserted. In this way, you avoid needlessly replacing good components.

CAUTION:

Extreme care should be taken when handling the integrated circuit chips. They are all very sensitive to static electricity and can easily be damaged ny careless handling. Always keep the chips in their plastic carrier tubes or on conductive foam when not handling them. Make certain you are well grounded when handling the chips.

In disassembly procedures, refer to Chapter 5 for reference.

6.2 SYMPTOM CHECKLIST

The symptom checklist is designed to give a rapid diagnosis for problems. The checklist preferred to be used by experienced service technician and for less experienced personnel, a step-by-step diagnosis flowchart is recommended.

Each symptom is accompanied by suitable replacements and remarks for references.

	SYMPTOM	REPLACEMENT / DIAGNOSIS	REMARKS
A.	No Power	Bad adaptor - PCB trace in power jack D1-D4 (1N5401)	 Over-use short circuit
	-12V	IC3 (7912), L2 (350uH Inductor)	Over-load
	+12V	IC2 (7812)	
	+ 5V	SD1 (1N5822)	
B.	No Colour	IC64 (MC1377) IC37 (V9938)	
C.	Poor Colour	Check power unit first Recalibrate VC3 for the clock frequency at 4.433 MHz for PAL (3.579 MHz for NTSC) Recalibrate VR1	 See figure 6.1 for reference See figure 6.2 for reference
D.	Cassette	Try another data cassette or tape	Incompatible with some other brands
	Save Problem	J12 (Relay), T3 (9014) IC52 (ULA9RA041)	Stop motor spinning
	Load Problem	IC38 (LM311) IC46 (AY-3-8910)	
E.	Printing	IC1 (74LS273) IC29 (74LS04) IC36 (7407)	Wrong connection short-circuit

F.	Poor Sound	IC9 (LM358)	
	No Music O/P	IC46 (AY-3-8910)	
	No Key Click O/P	IC52 (ULA9RA041)	
G.	Keyboard	Use test cartridge to identify individual opened / shorted key switch(es)	Refer to keyboard diagnostic flowchart
	No Response	Check the connection flex cable IC52 (ULA9RA041)	
H.	Fails to Boot Cartridge	IC30, IC31 (74LS244) IC26 (74LS367) IC33 Z80A IC35 (ULA5RA087) IC52 (ULA9RA041) IC51 (23256)	Probably caused by inserting / removing cartridge having power ON
I.	Joystick (I/O) Port Failure	IC47 (74LS157) IC48 (74LS157) IC36 (7407) IC46 (AY-3-8910)	Port 1 Port 2 Port 1 and 2
J.	RS-232C Port Failure	IC8 (1488) IC7 (1489) IC11 (8251A) IC12 (8253) XT1 (1.8432 MHz)	See figure 6.3
K.	Disk Failure	Refer to diagnostic flowchart	
L.	Boot Up Failure	Refer to diagnostic flowchart	

6.3 DIAGNOSTIC FLOWCHART FOR SVI-728 COMPUTER

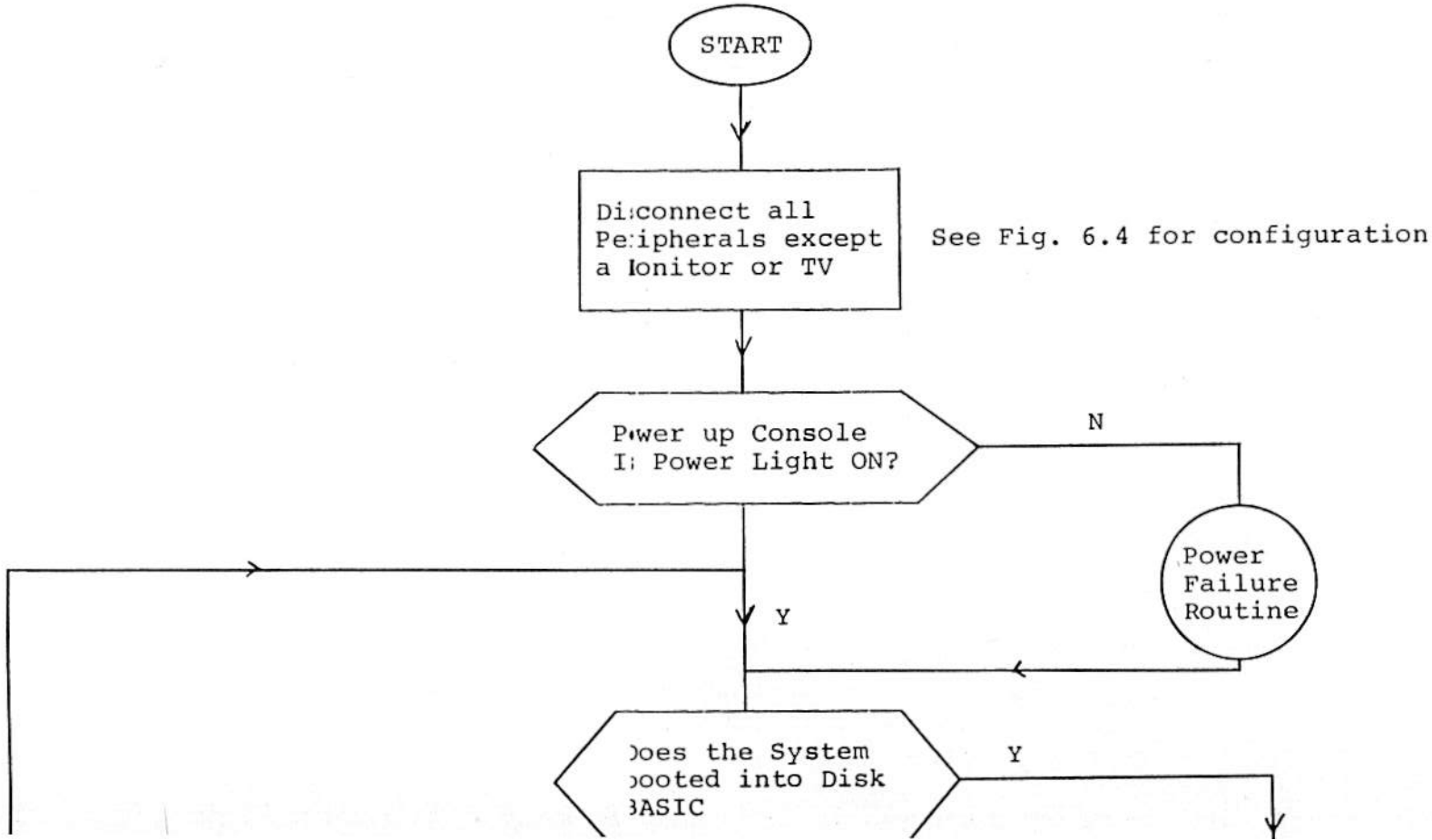
The Diagnostic Flowchart is intended to be easy to use and the primary aid when troubleshooting the SVI-738 computer console. This flowchart is meant to be used with a test cartridge. Follow the flows in the order presented. A simple 'Yes' or 'No' decision in the flowchart would direct user to faulty area.

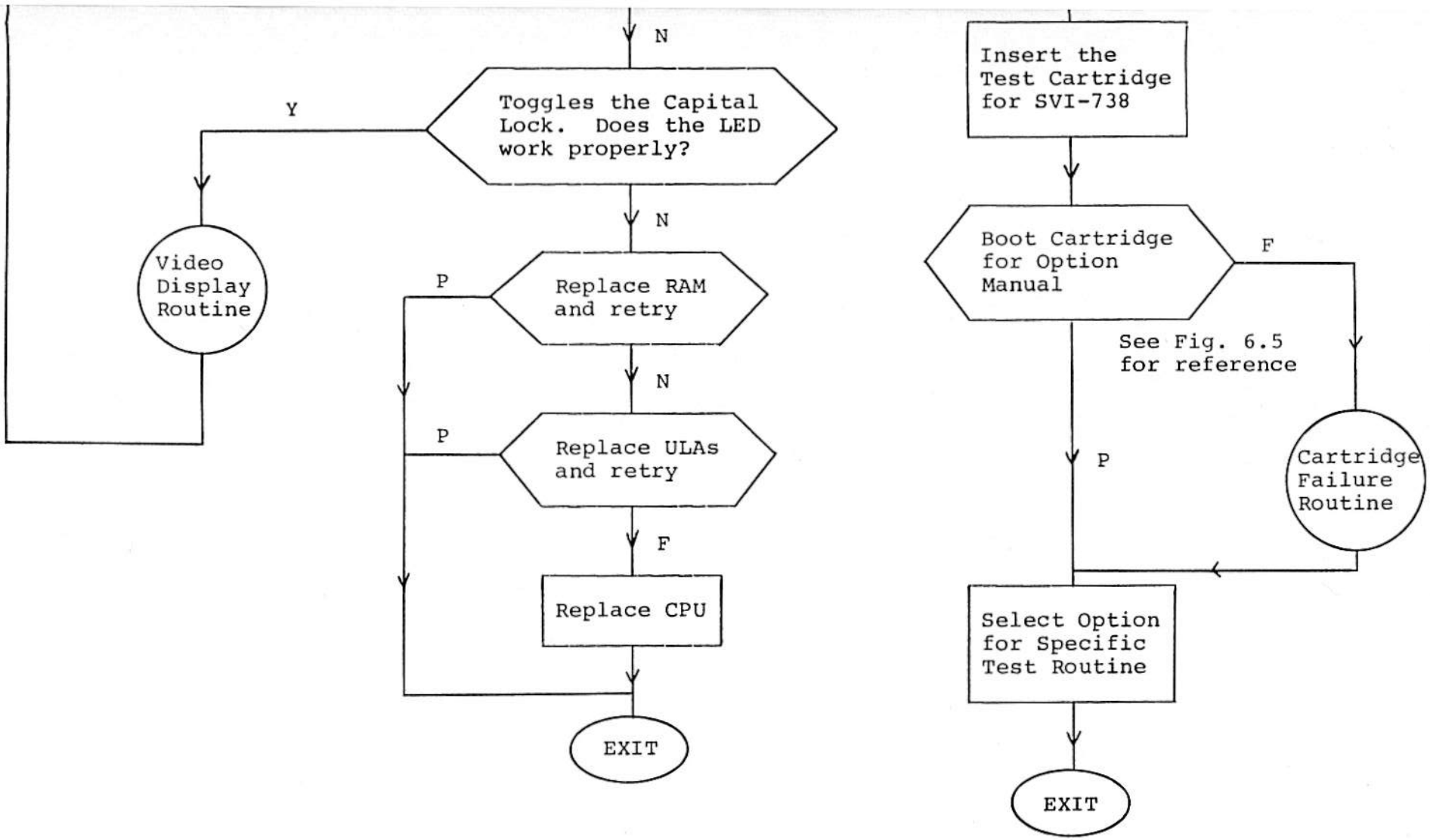
Tens of test points (TP1-TP20) are installed in the circuit board and together with the relevant waveform diagram in this chapter, it provides you a easy access to trouble area or IC(s).

In case the Diagnostic Flowchart does not solve your problem, please consult experience repairman or your local agency for further advice and evaluation.

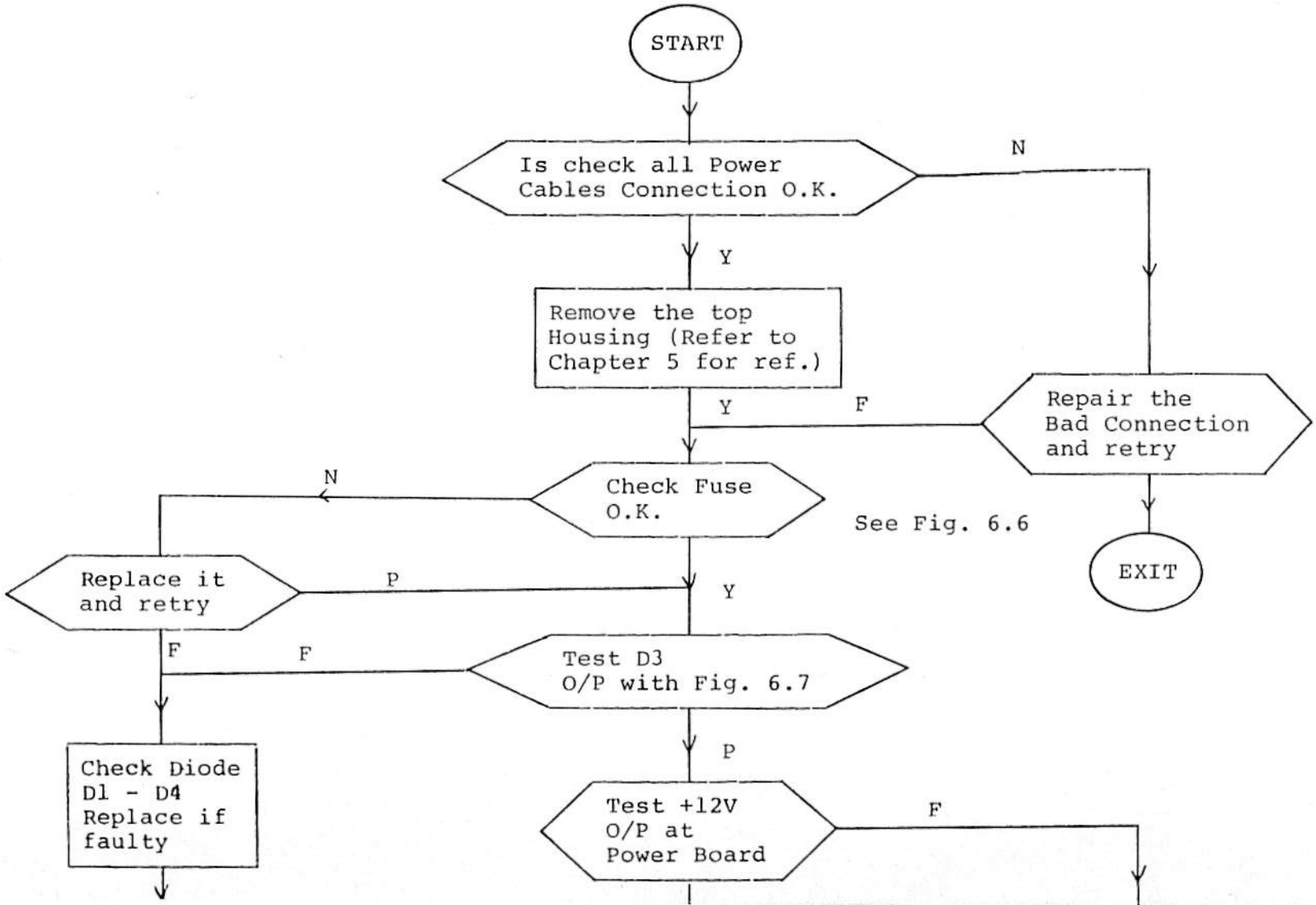
6.3.1 BASIC OPERATION CHART

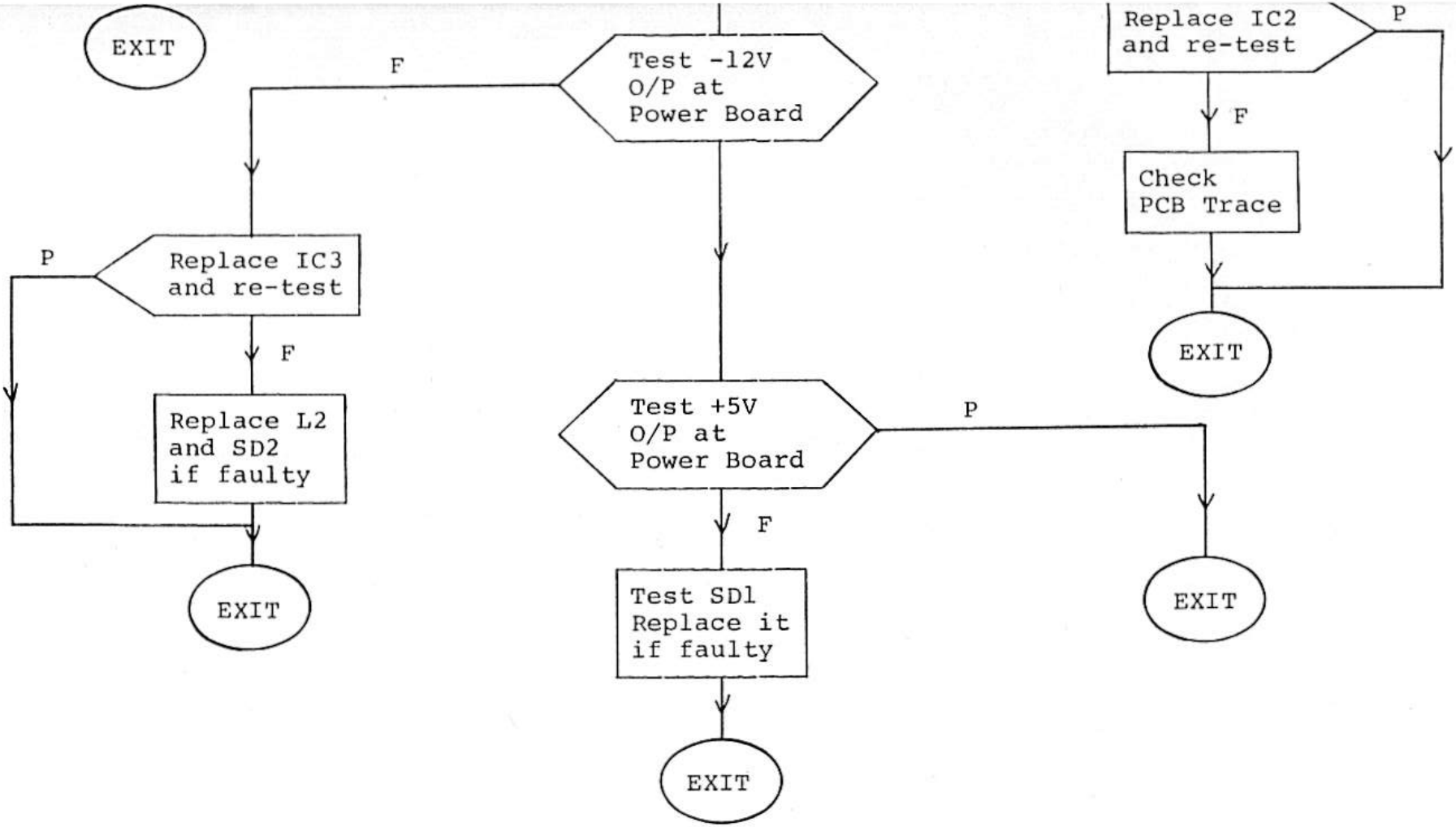
*F - Test Fails or Unexpected Results
*P - Test Pass
*Y - Yes to Question Asked
*N - No to Question Asked



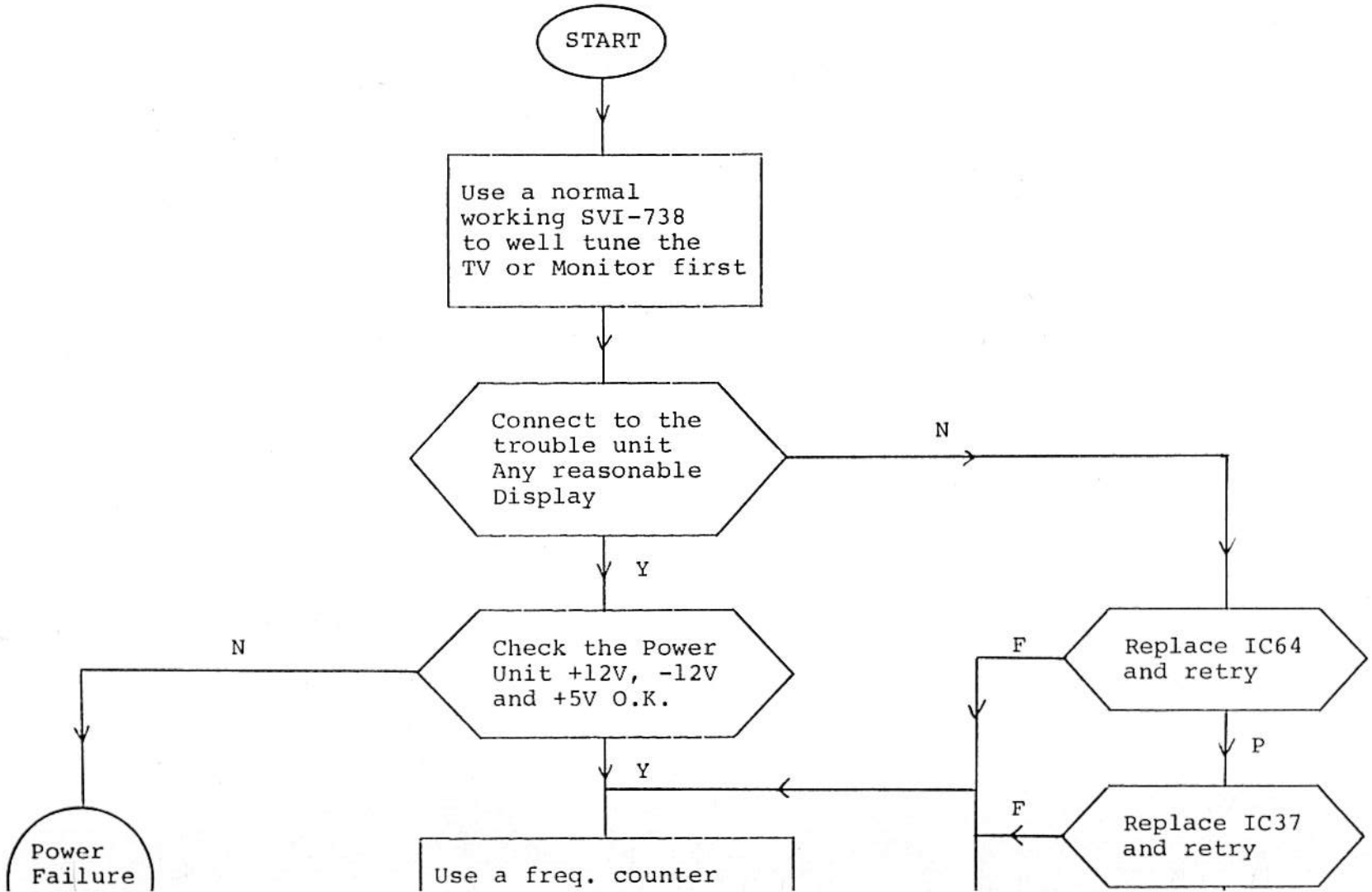

N
Toggles the Capital Lock. Does the LED work properly?
Y
Video Display Routine
N
P
Replace RAM and retry
N
P
Replace ULAs and retry
F
Replace CPU
EXIT
Insert the Test Cartridge for SVI-738
Boot Cartridge for Option Manual
F
See Fig. 6.5 for reference
P
Cartridge Failure Routine
Select Option for Specific Test Routine
EXIT

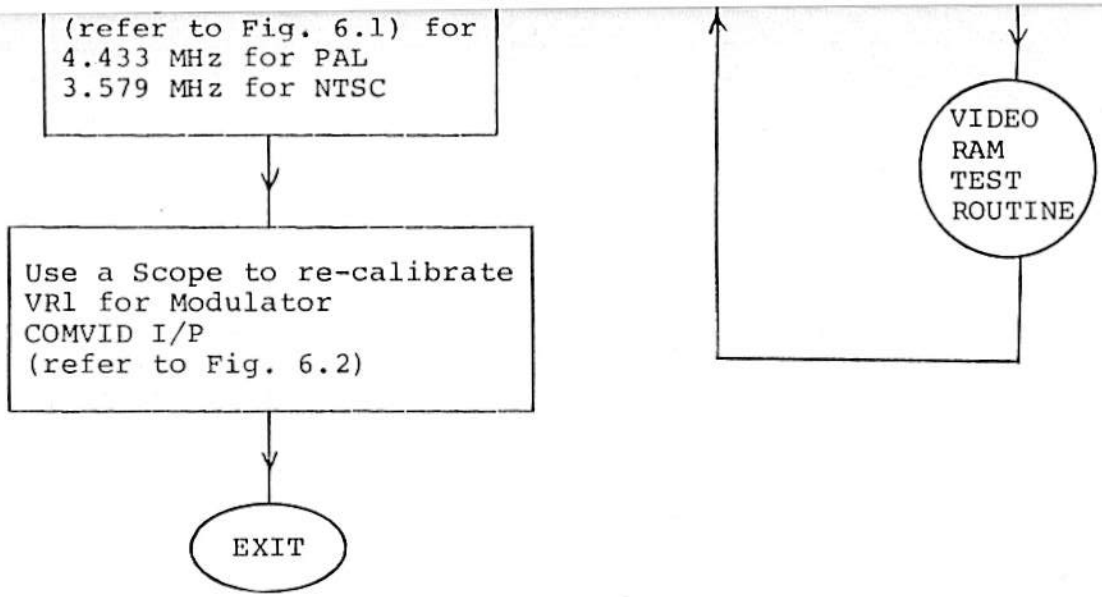
6.3.2 POWER FAILURE RECOVER ROUTINE



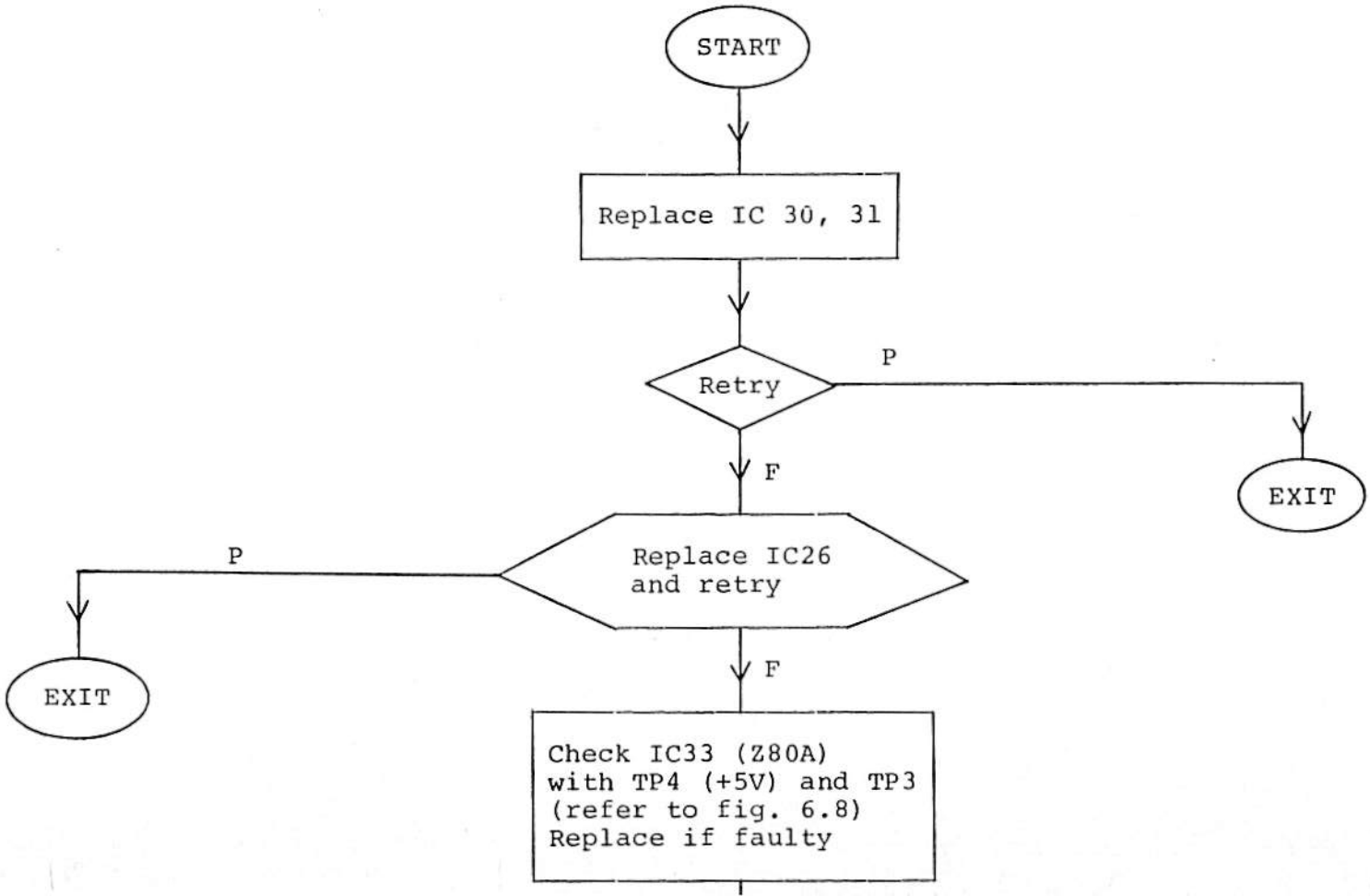

EXIT
F
Test -12V
O/P at
Power Board
Replace IC2
and re-test
P
F
Check
PCB Trace
EXIT
P
Replace IC3
and re-test
F
Replace L2
and SD2
if faulty
EXIT
Test +5V
O/P at
Power Board
P
F
Test SD1
Replace it
if faulty
EXIT
EXIT

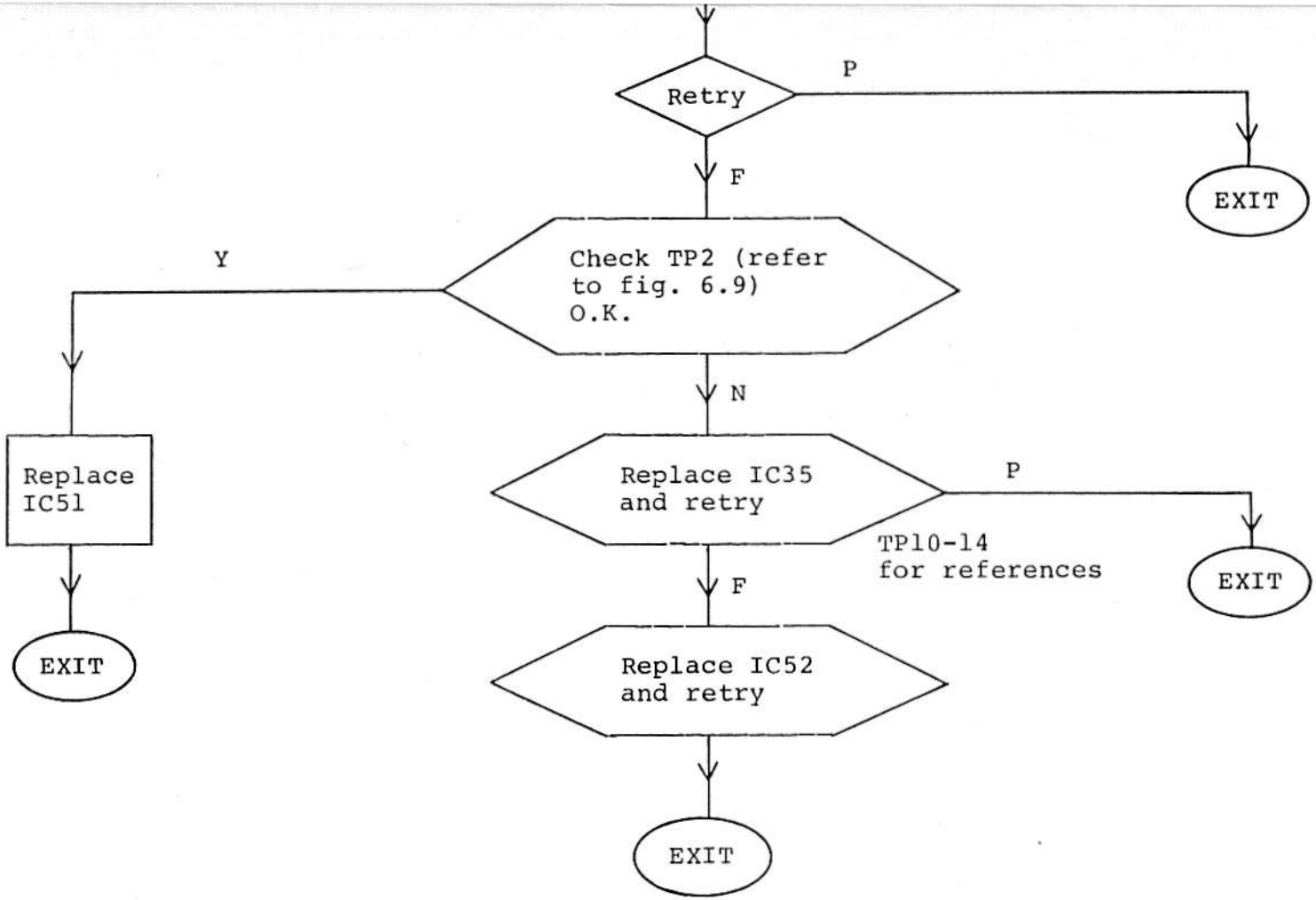
6.3.3 VIDEO DISPLAY RECOVER ROUTINE



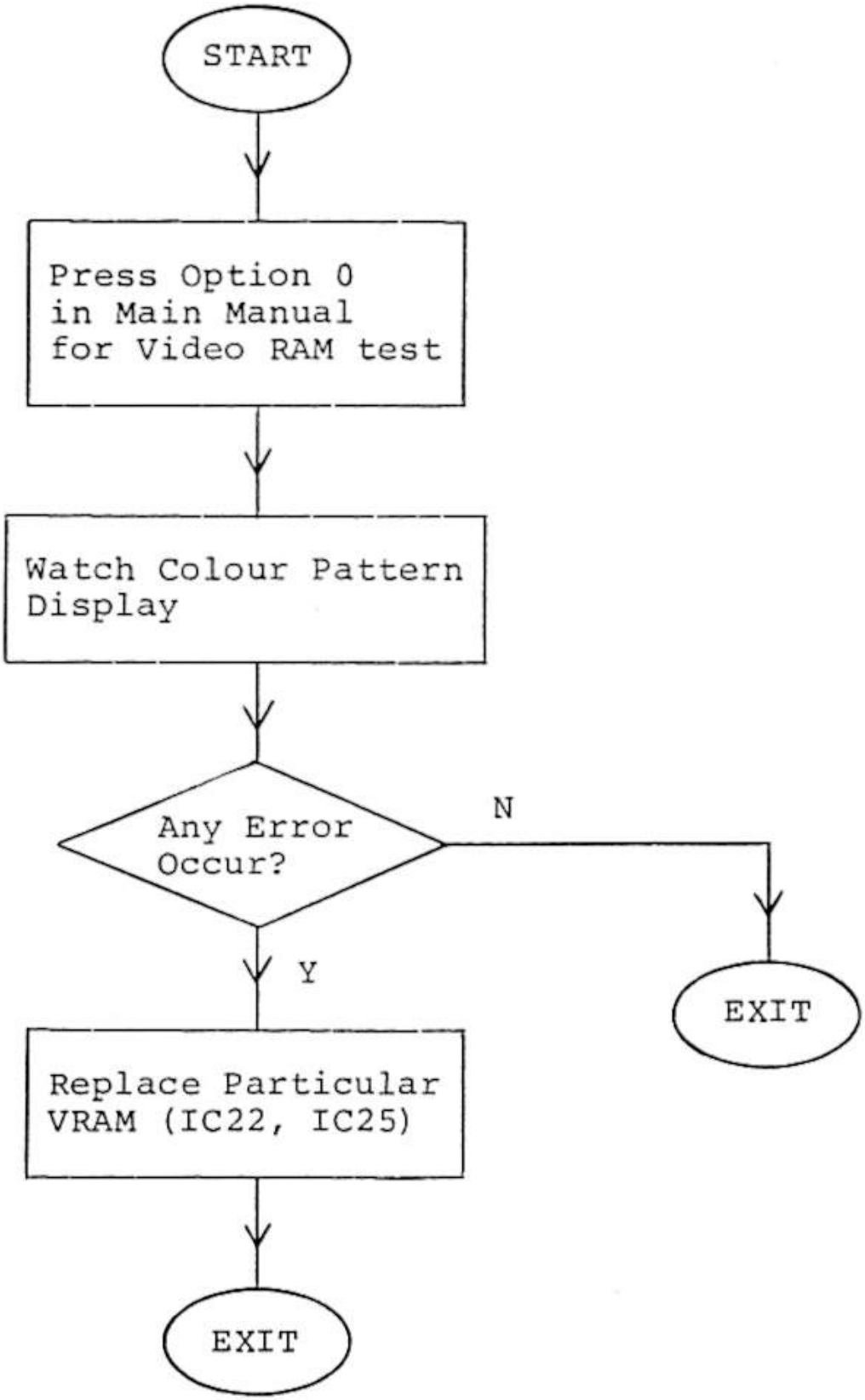

(refer to Fig. 6.1) for
4.433 MHz for PAL
3.579 MHz for NTSC
Use a Scope to re-calibrate
VR1 for Modulator
COMVID I/P
(refer to Fig. 6.2)
EXIT
VIDEO
RAM
TEST
ROUTINE

6.3.4 CARTRIDGE BOOT-UP FAILURE RECOVER ROUTINE

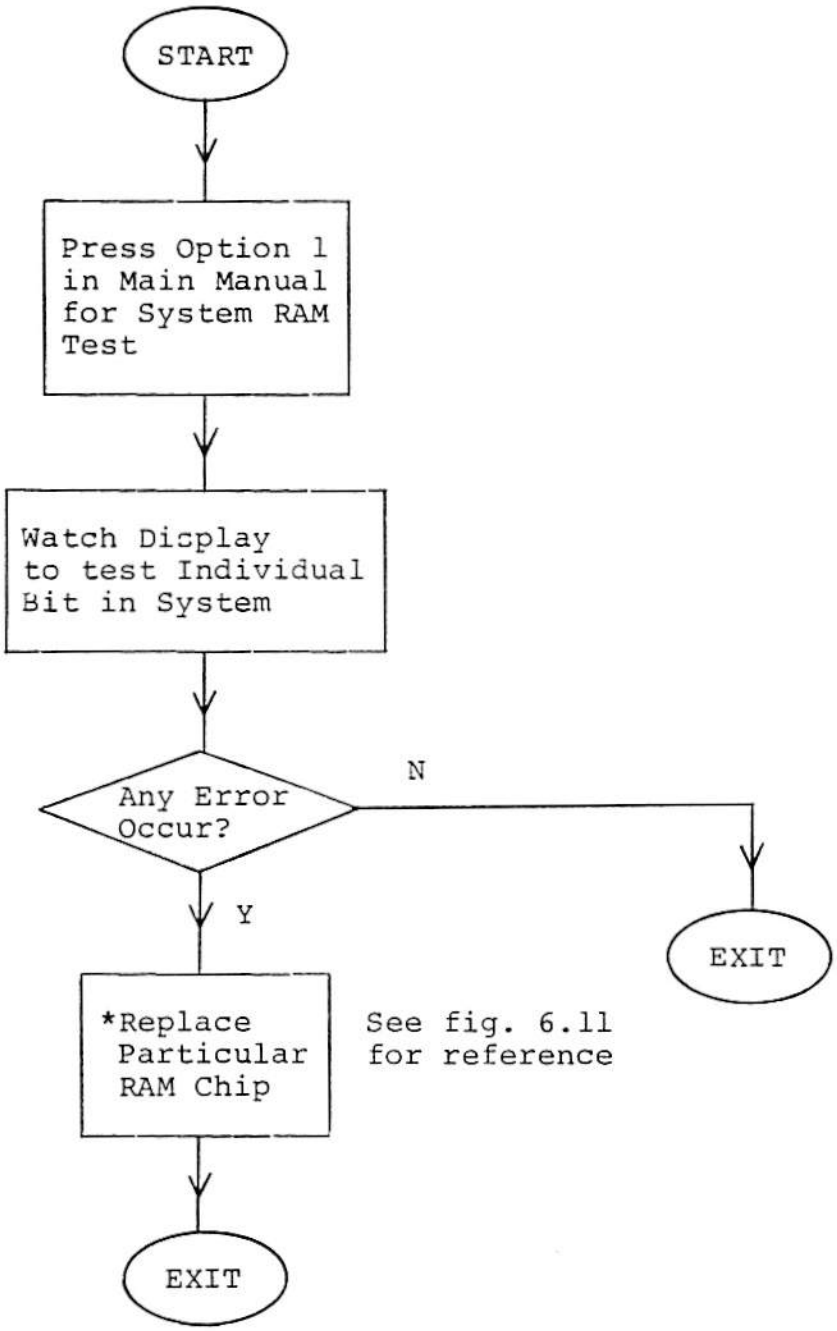



Retry
P
EXIT
F
Check TP2 (refer to fig. 6.9) O.K.
Y
N
Replace IC51
EXIT
Replace IC35 and retry
P
TP10-14 for references
EXIT
F
Replace IC52 and retry
EXIT

6.3.5 VIDEO RAM TEST ROUTINE

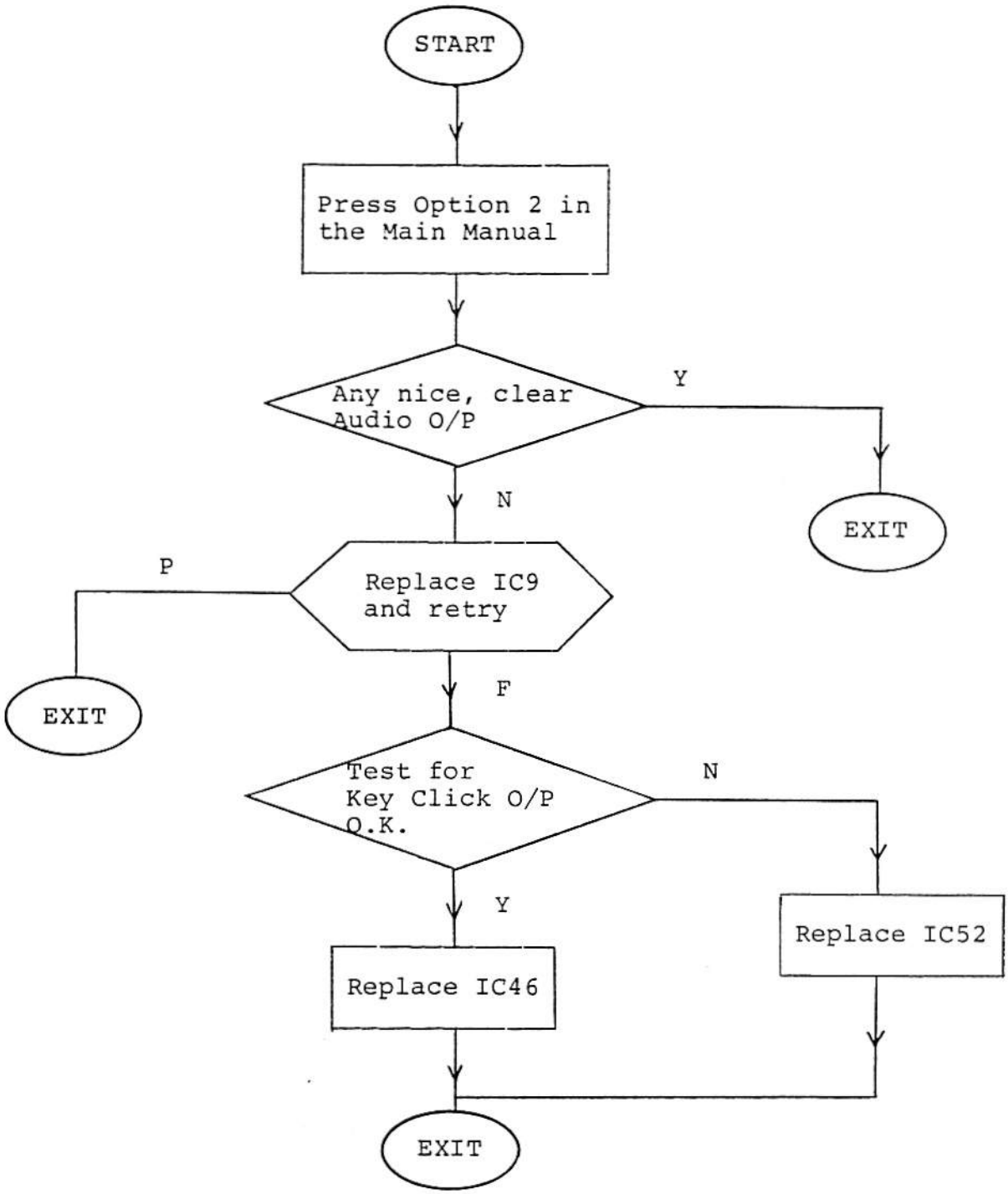


6.3.6 SYSTEM RAM TEST ROUTINE

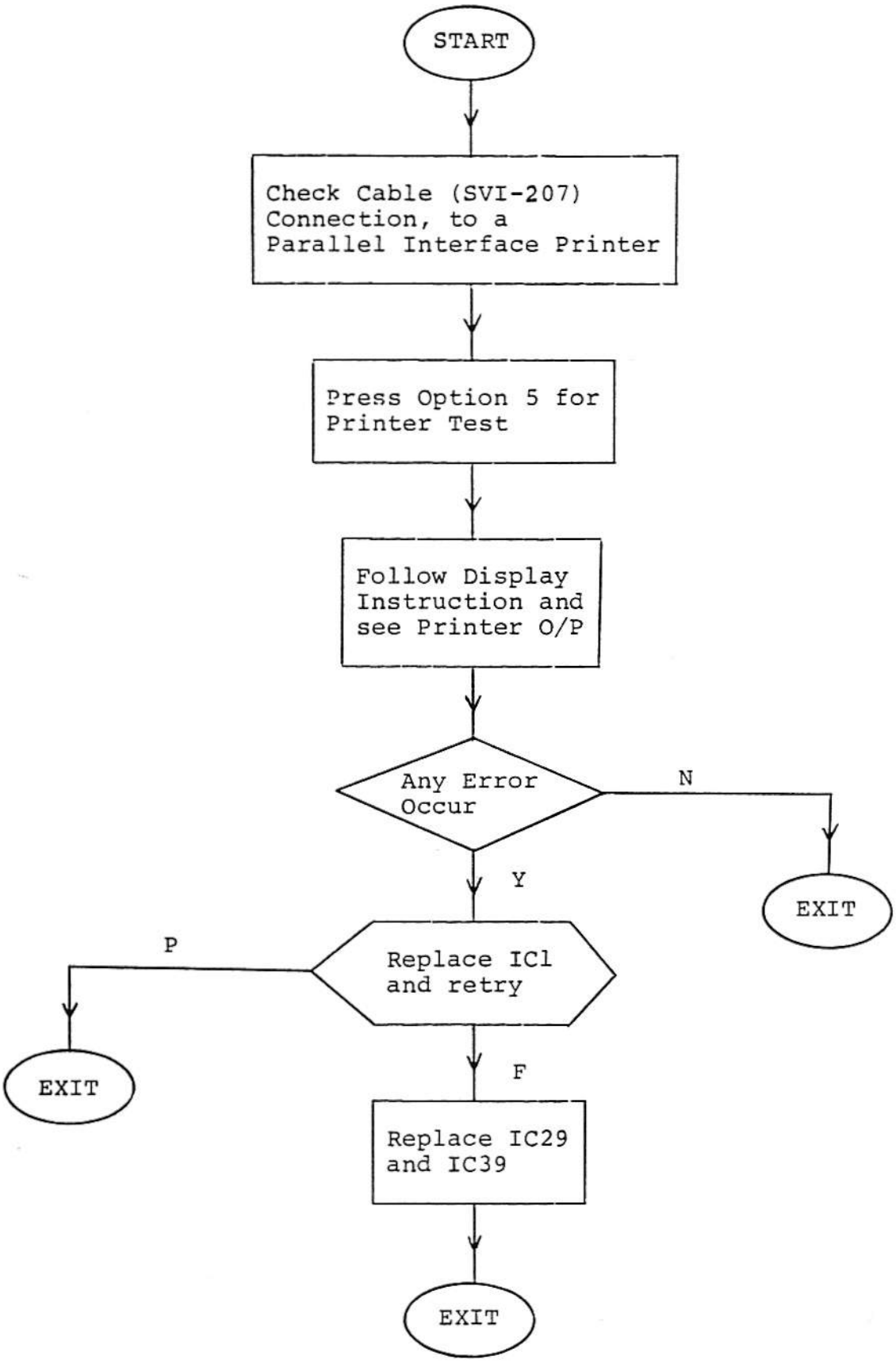


* In some case (more than 1 error bit), and RAMs (IC53-IC60) need to be replaced.

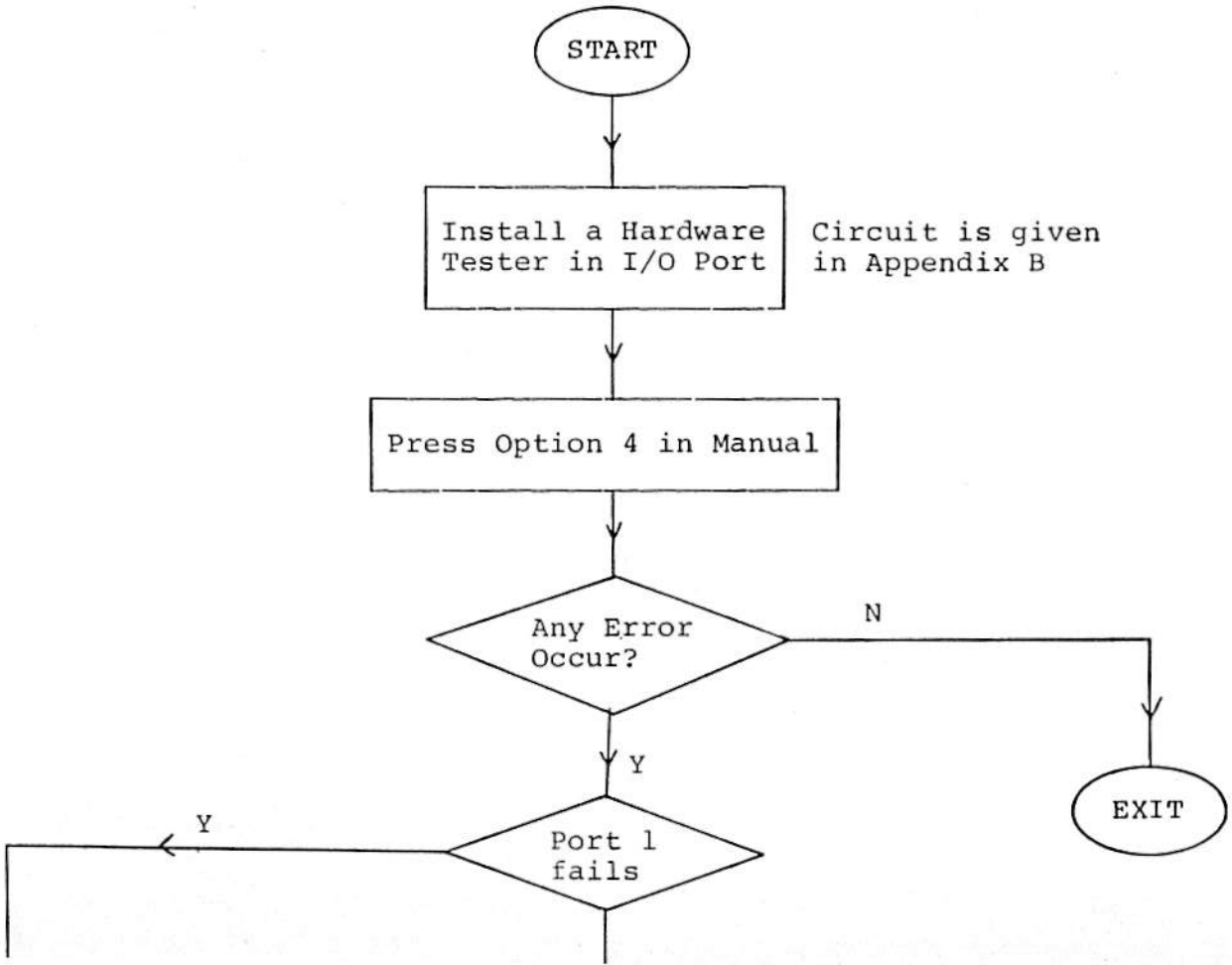
6.3.7 PSG AND SOUND TEST ROUTINE

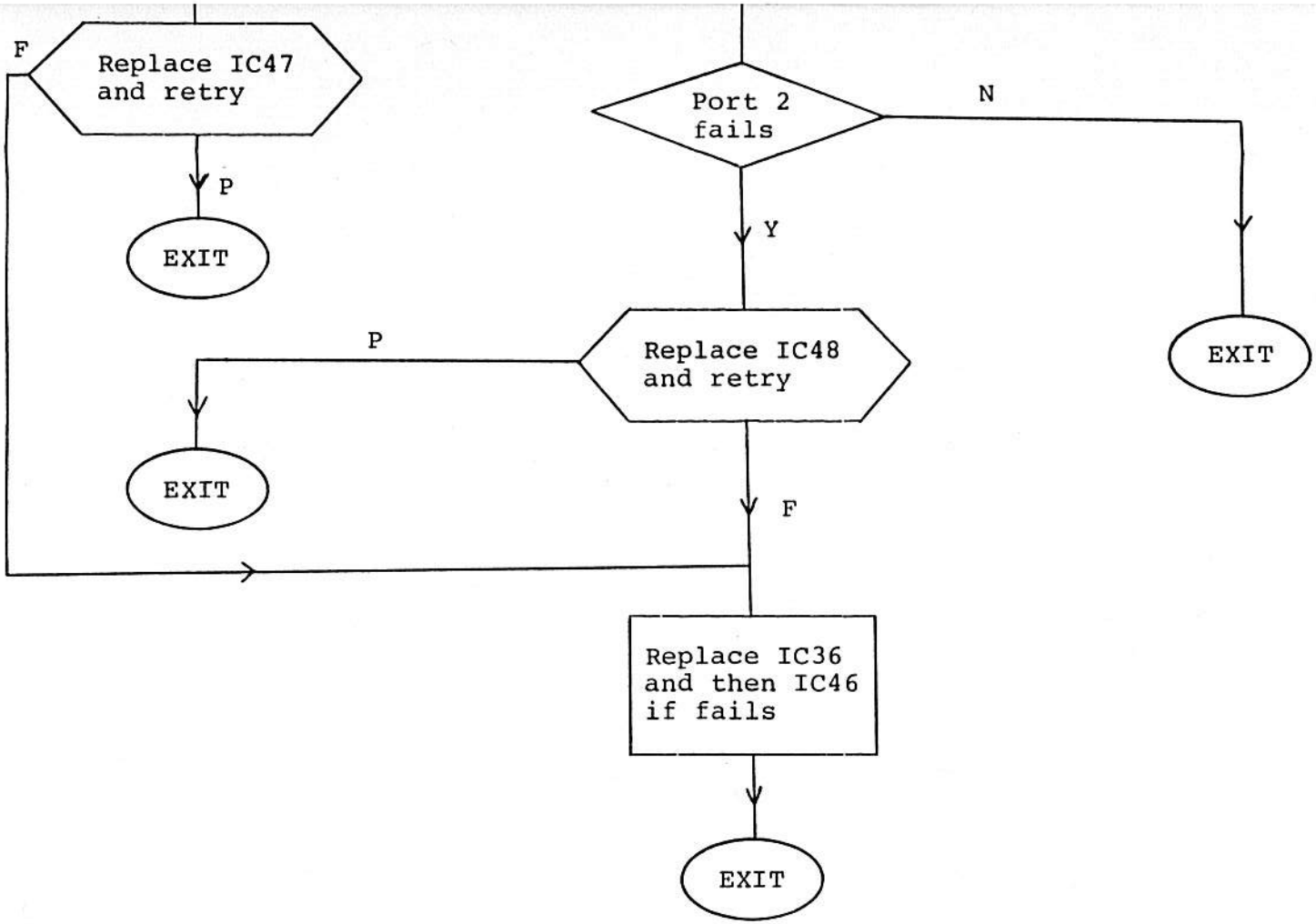


6.3.8 PRINTING TEST ROUTINE

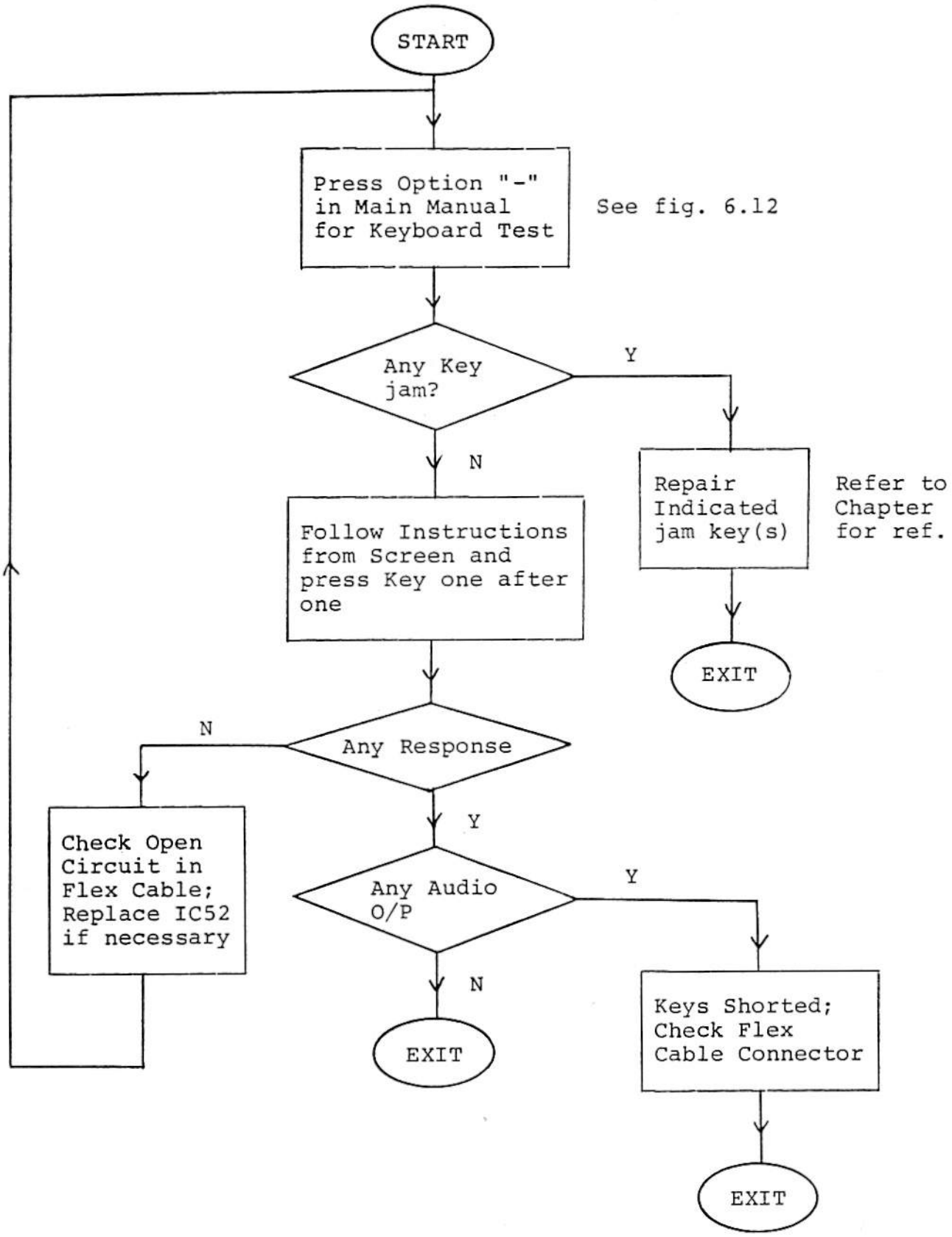


6.3.9 JOYSTICK (I/O) PORT TEST




F
Replace IC47
and retry
P
EXIT
Port 2
fails
N
Y
EXIT
P
Replace IC48
and retry
EXIT
F
Replace IC36
and then IC46
if fails
EXIT

6.3.10 KEYBOARD ROUTINE TEST



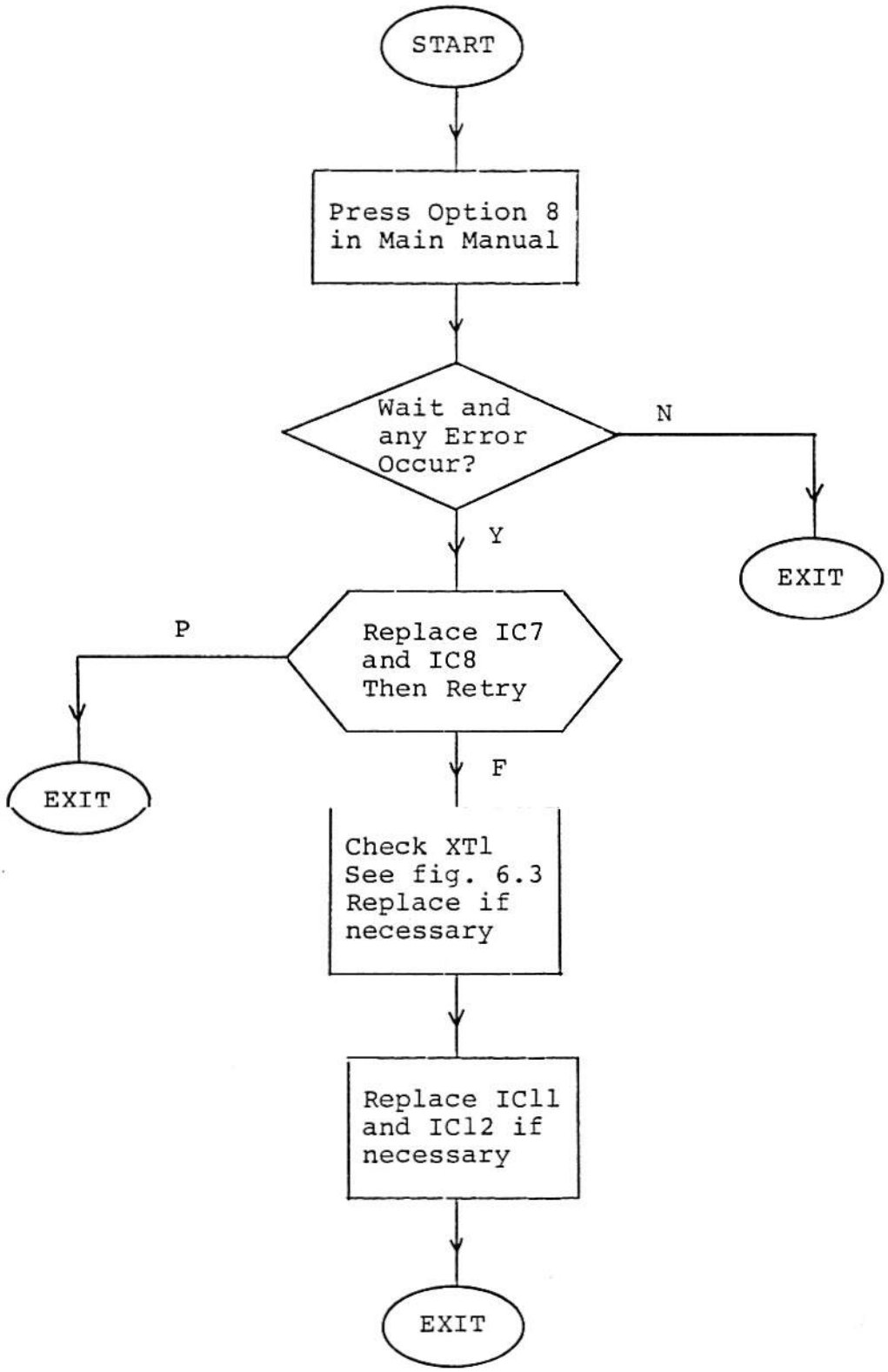
6.3.11 SYSTEM ROM TEST ROUTINE

Checksum of system ROM is tested under test cartridge programme (option 6 in Main Manual). If any error occurs, replaces system ROM (IC51 23256).

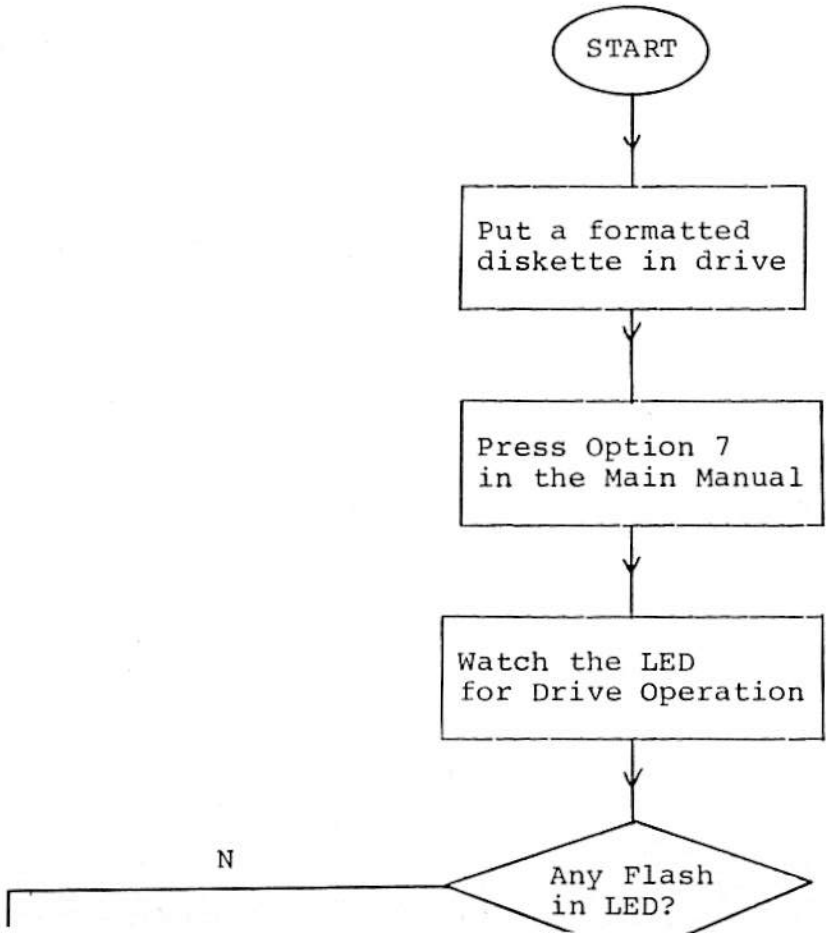
Remember - the 1.3 version test cartridge only suitable for International (INT), Germany (DIN) and Swedish or Finnish version machines.

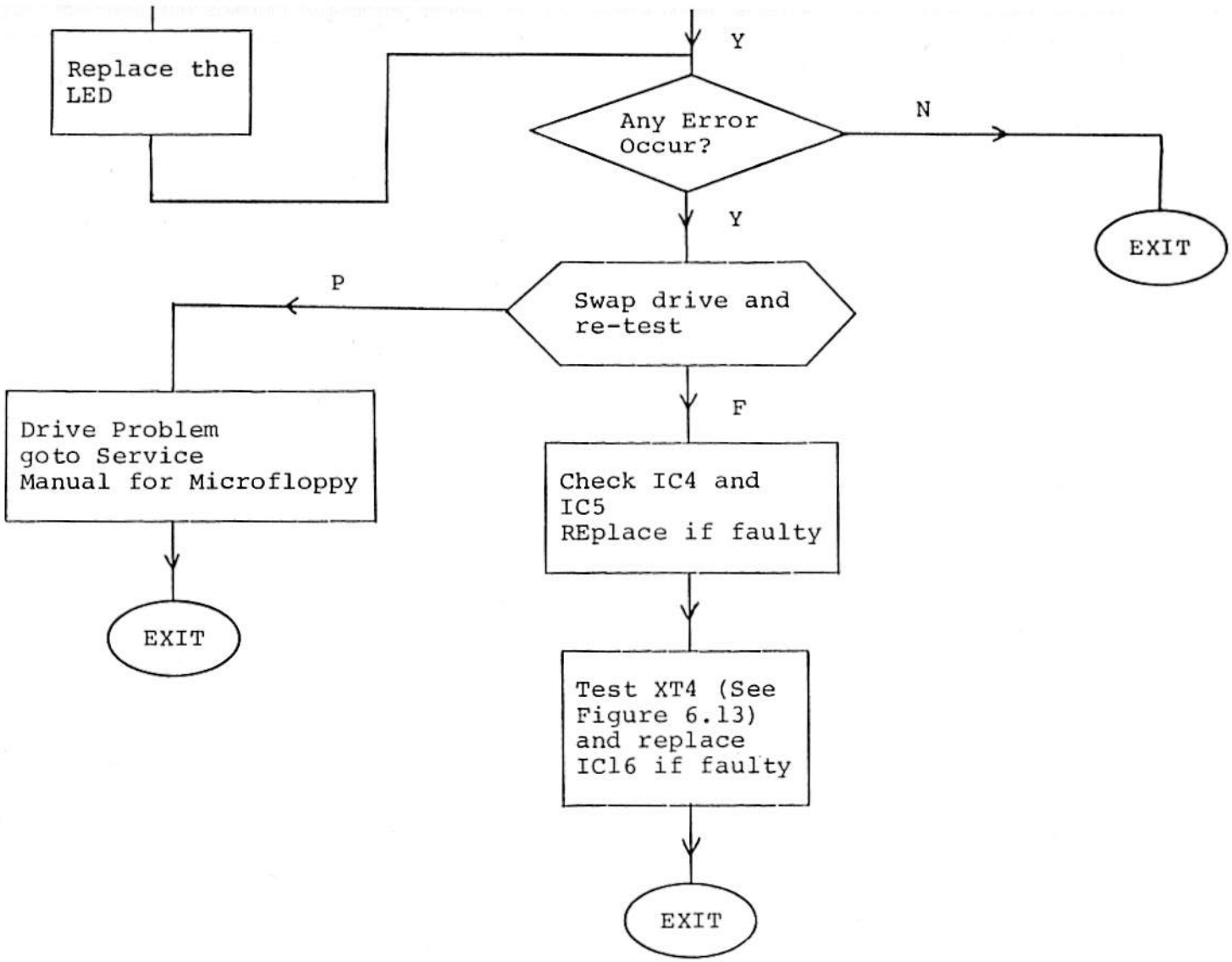
6.3.12 RS-232 PORT TEST ROUTINE

To perform the self test for RS-232C interface, connect Pin 2 and Pin 3 together and then Pin 4 to Pin 5 of RS-232C port.

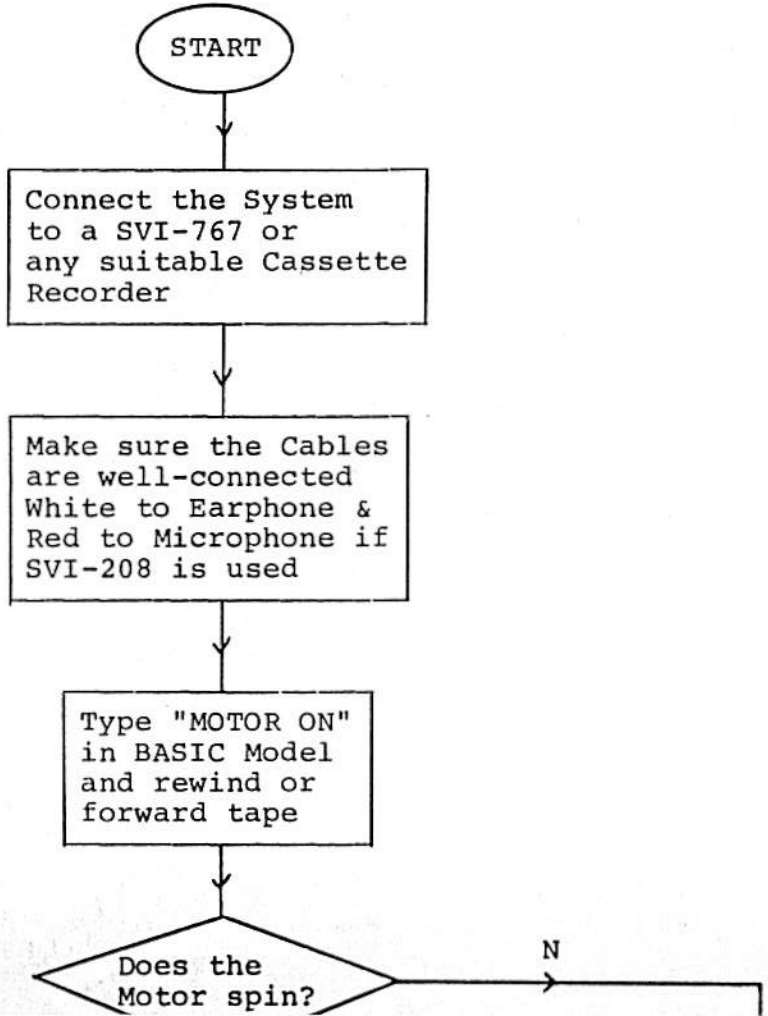


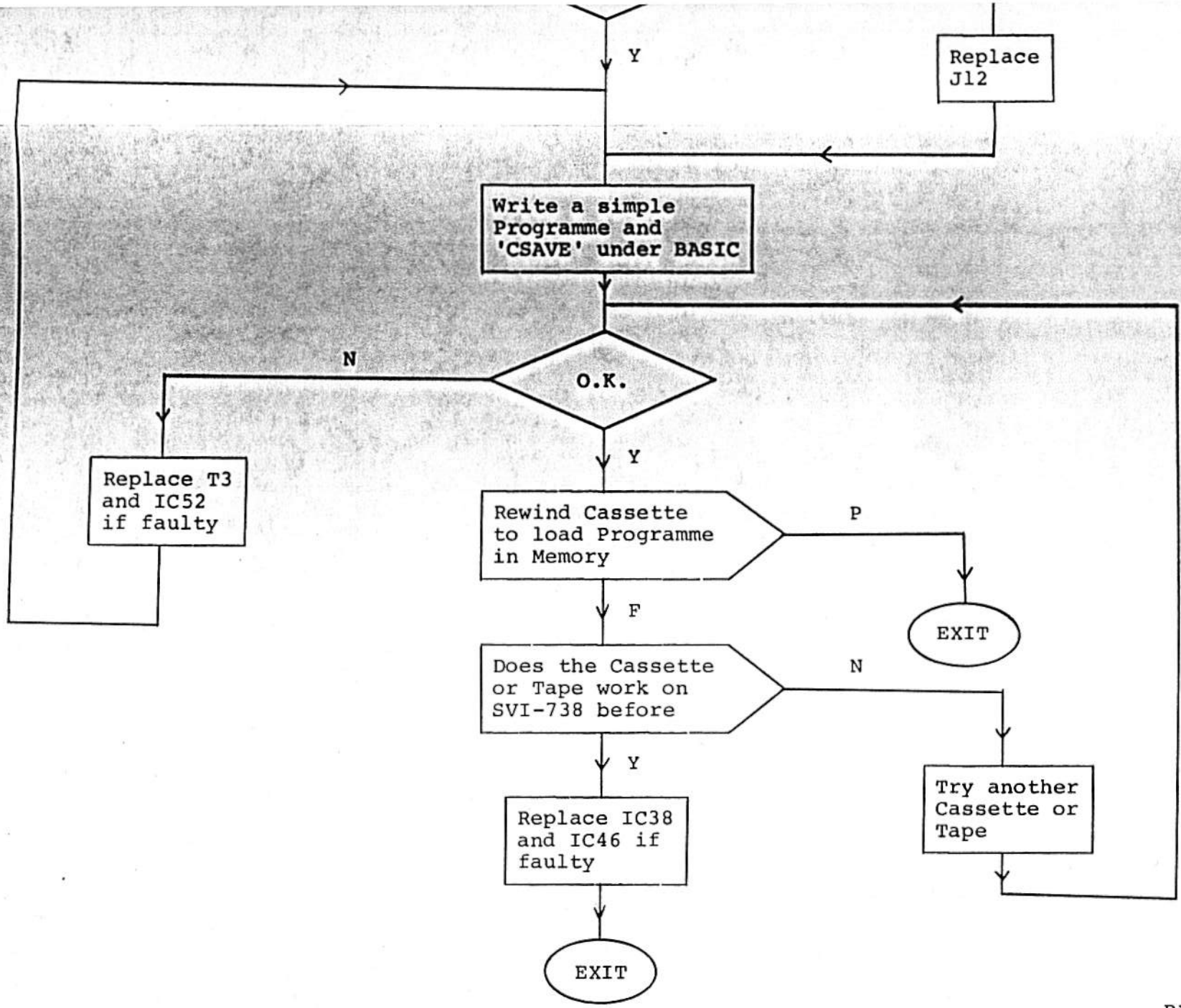
6.3.13 DISK DRIVE INTERFACE TEST ROUTINE




Replace the LED
Y
Any Error Occur?
N
EXIT
Y
Swap drive and re-test
P
Drive Problem goto Service Manual for Microfloppy
EXIT
F
Check IC4 and IC5 REplace if faulty
Test XT4 (See Figure 6.13) and replace IC16 if faulty
EXIT

6.3.14 CASSETTE PORT TEST ROUTINE




Y
Replace J12
Write a simple Programme and 'CSAVE' under BASIC
N
O.K.
Y
Replace T3 and IC52 if faulty
Rewind Cassette to load Programme in Memory
P
EXIT
F
Does the Cassette or Tape work on SVI-738 before
N
Y
Try another Cassette or Tape
Replace IC38 and IC46 if faulty
EXIT

6.4 REFERENCE FIGURES OR PHOTOGRAPHS FOR TROUBLE SHOOTING

Note: A X10 probe is used for taking signal waveform

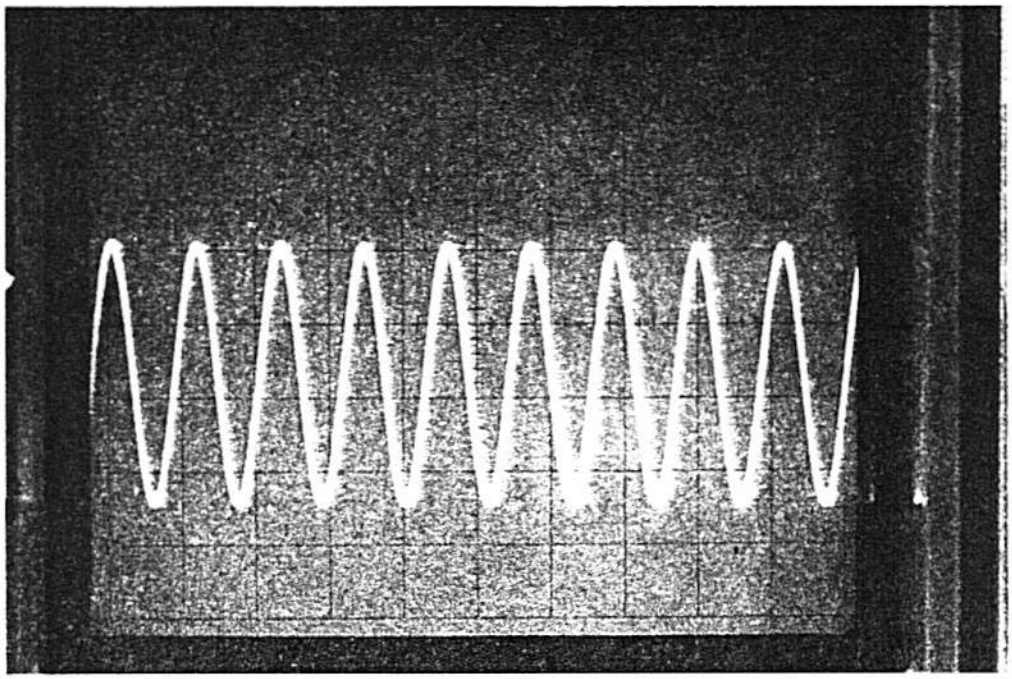


Figure 6.1 IC64 (RF) Clock Frequency 4.433 MHz for PAL Version (3.579 MHz for NTSC Version); 0.2us/div 0.2v/div

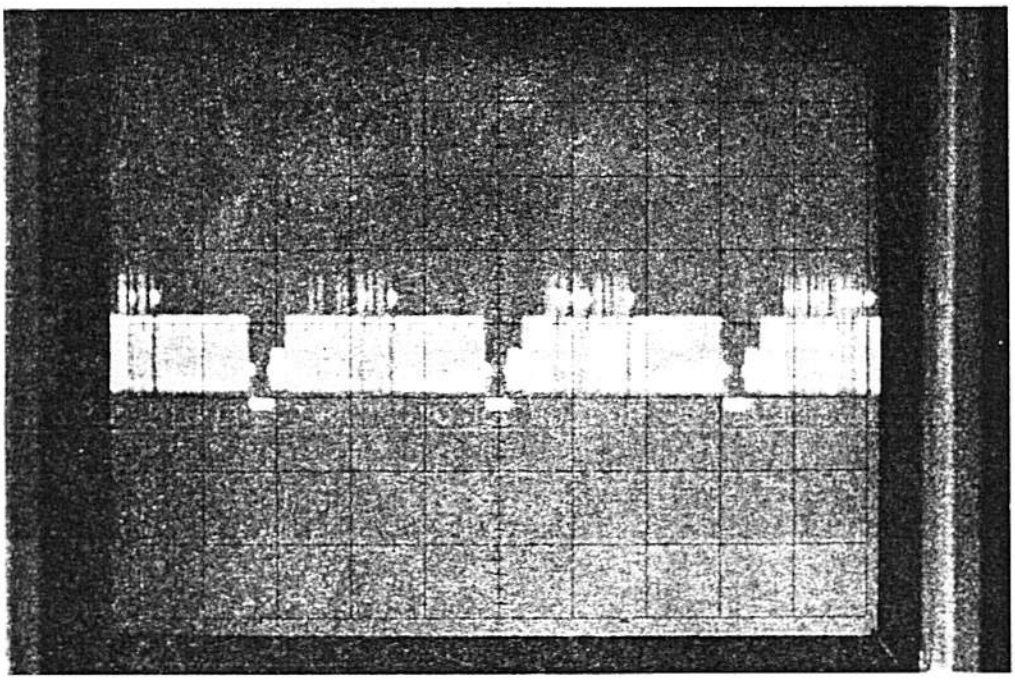


Figure 6.2 Modulator Composite Video (VR1) O/P; 0.5msec/div 5mv/div

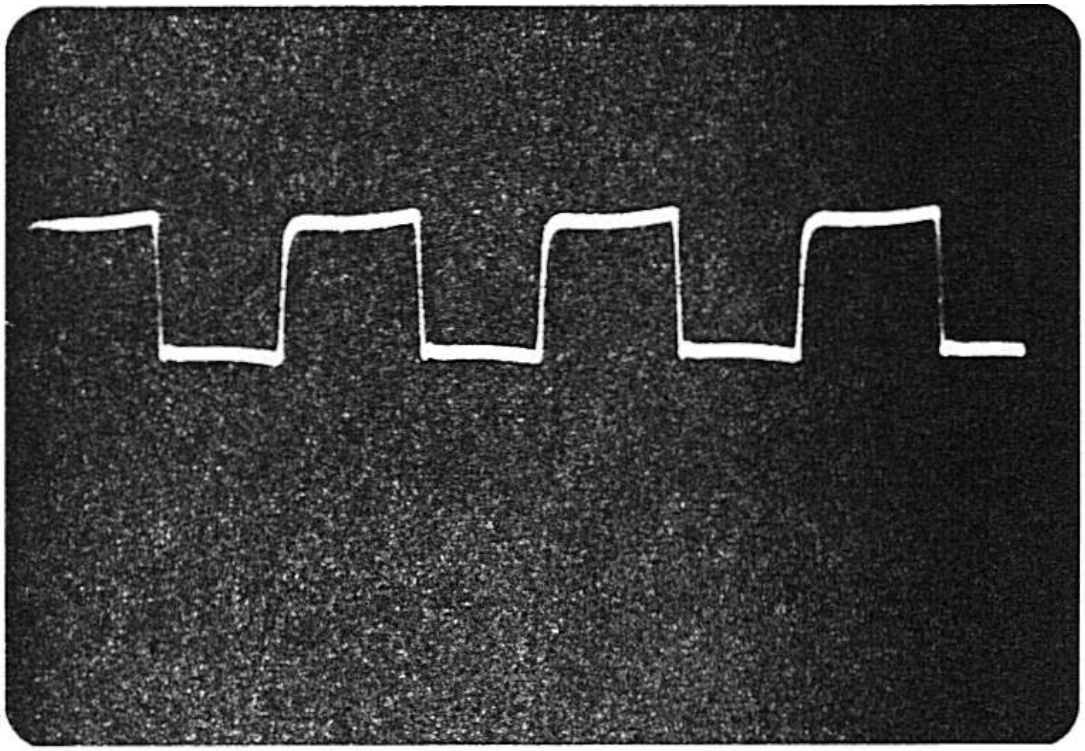


Figure 6.3 RS-232C Interface Clock Frequency (XT1)
1.843MHz; 0.2usec/div 0.2v/div

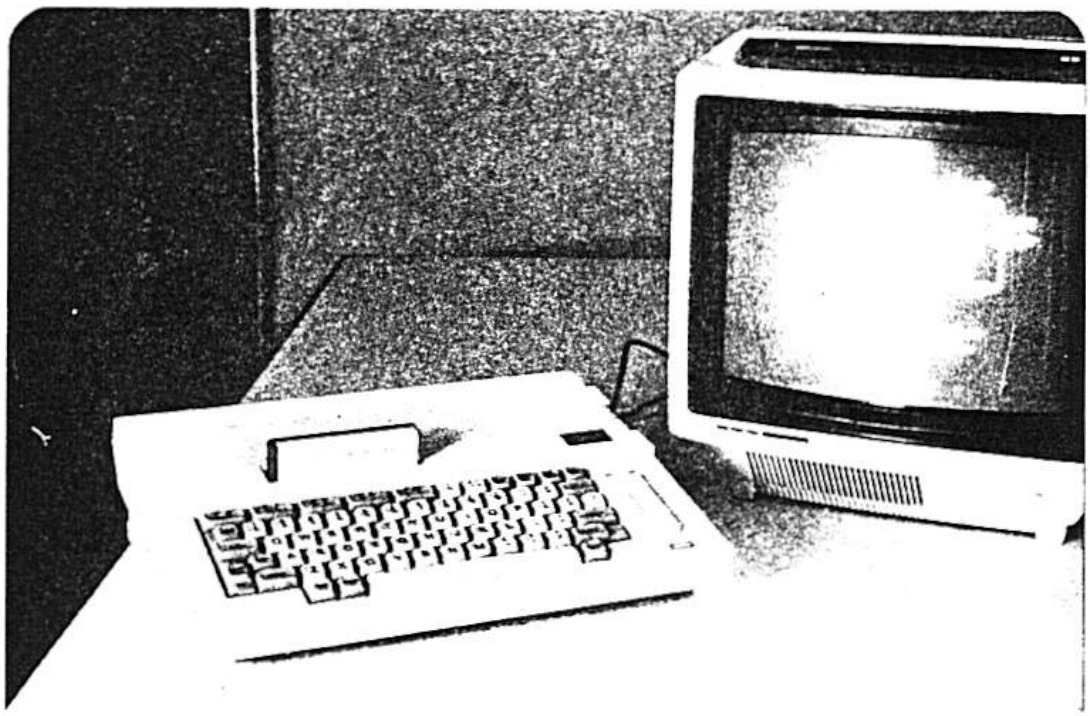
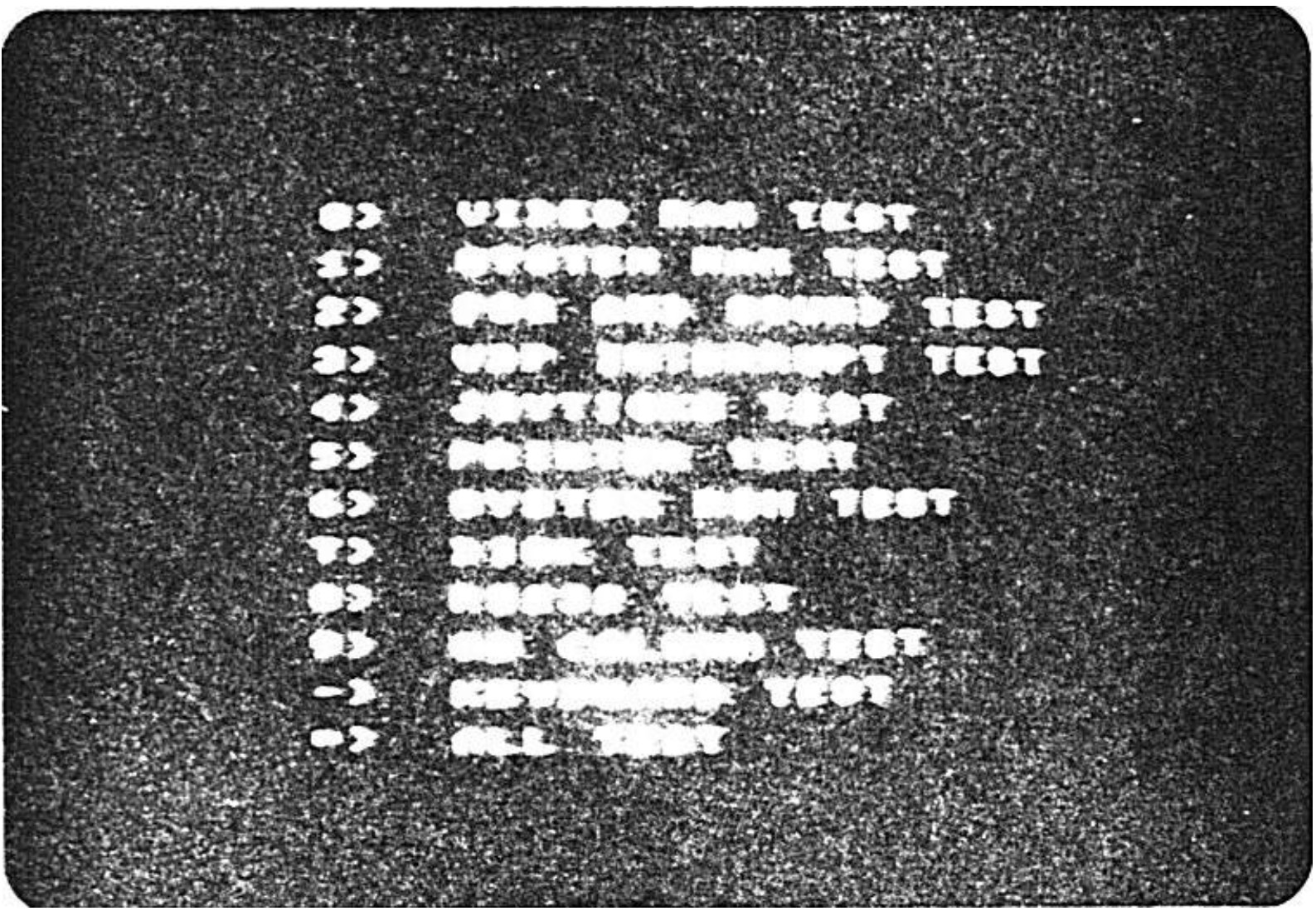


Figure 6.4 Basic Diagnostic Configuration



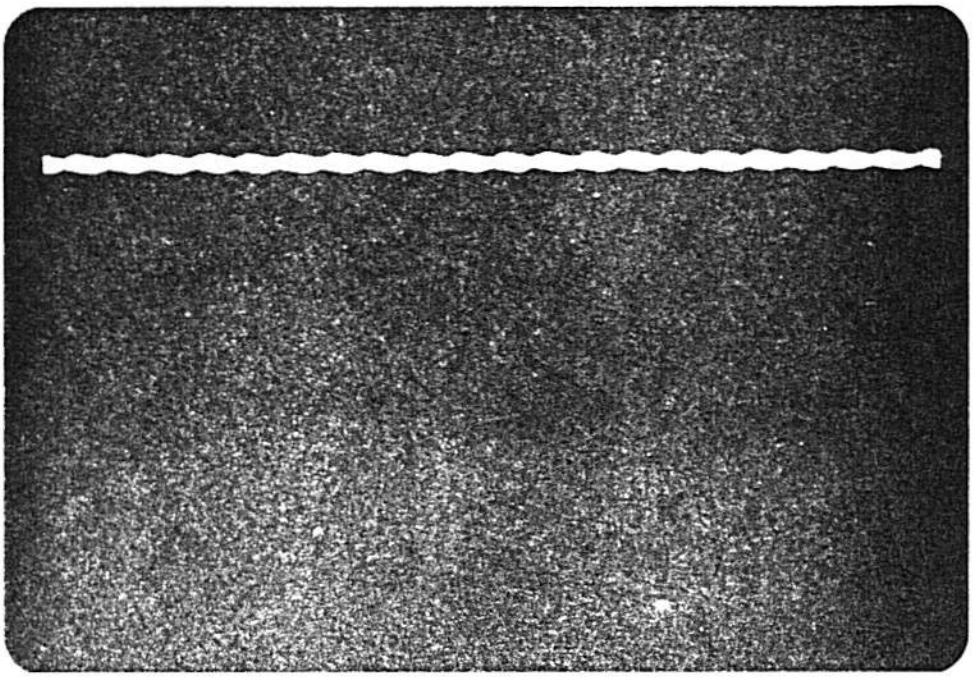


Figure 6.7 Rectified Voltage O/P (Power Board D3 O/P);
10msec/div 1v/div

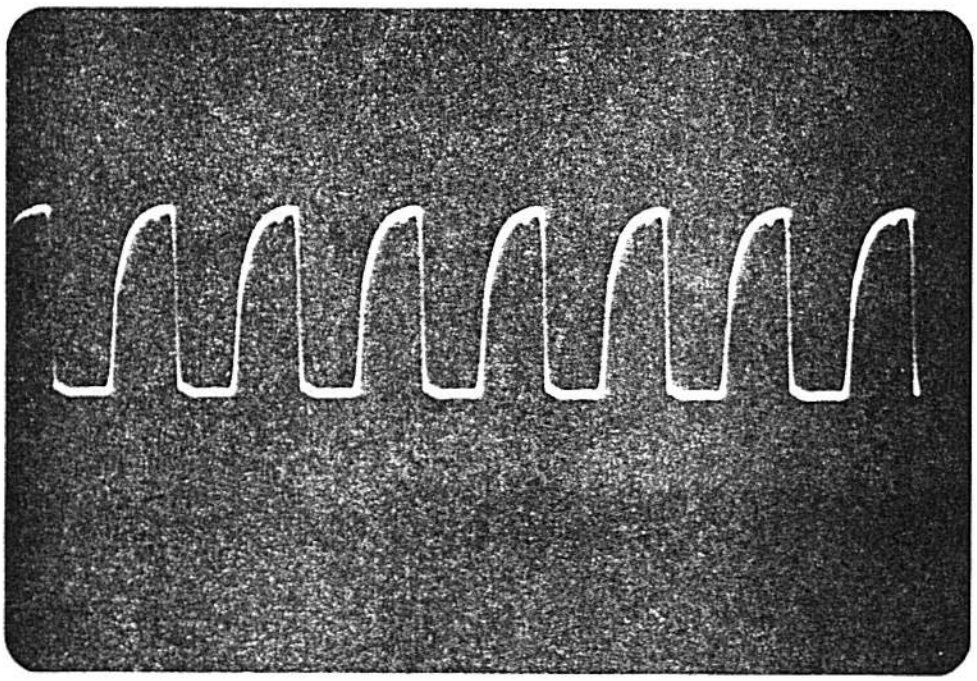


Figure 6.8 CPU (Z80A) Clock Frequency (TP3) 3.579MHz;
0.2use/div 0.2v/div

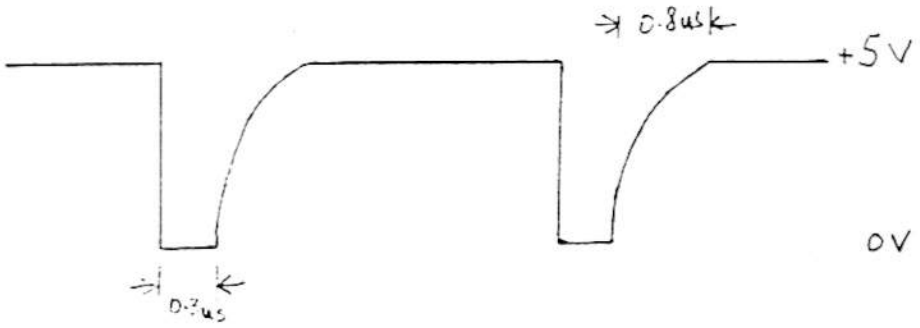


Figure 6.9 CPU $\overline{\text{WAIT1}}$ Cycle Waveform (TP2); 0.5usec/div 0.2v/div

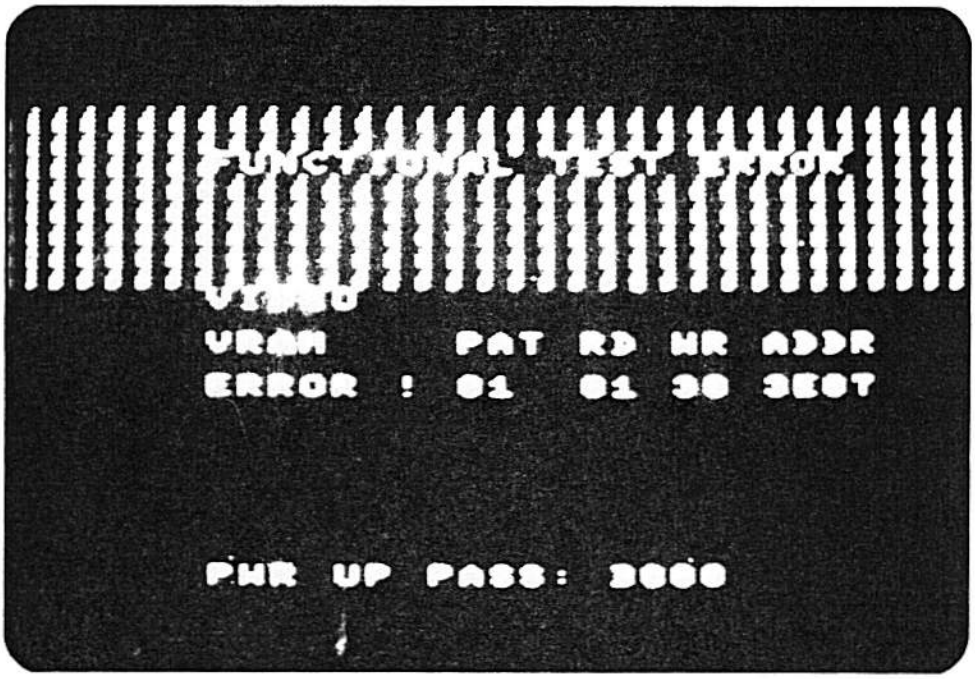


Figure 6.10 VRAM Error Display
Replace IC22, IC25 (4416 RAM)

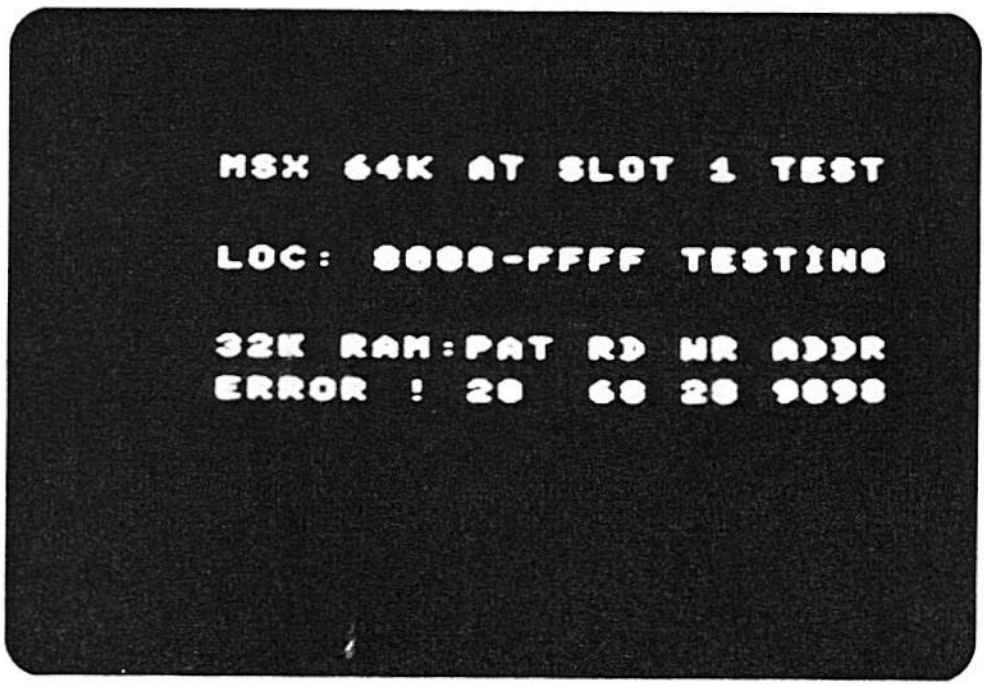


Figure 6.11 System RAM Error Display

Error Location:

Bit No.	7	6	5	4	3	2	1	0
RD Content ---> WR Content --->	0 0	1 0 ↑ Error Bit	1 1	0 0	1 1	0 0	0 0	0 0
IC number to be replaced if error occurs	IC60	IC59	IC58	IC57	IC56	IC55	IC54	IC53

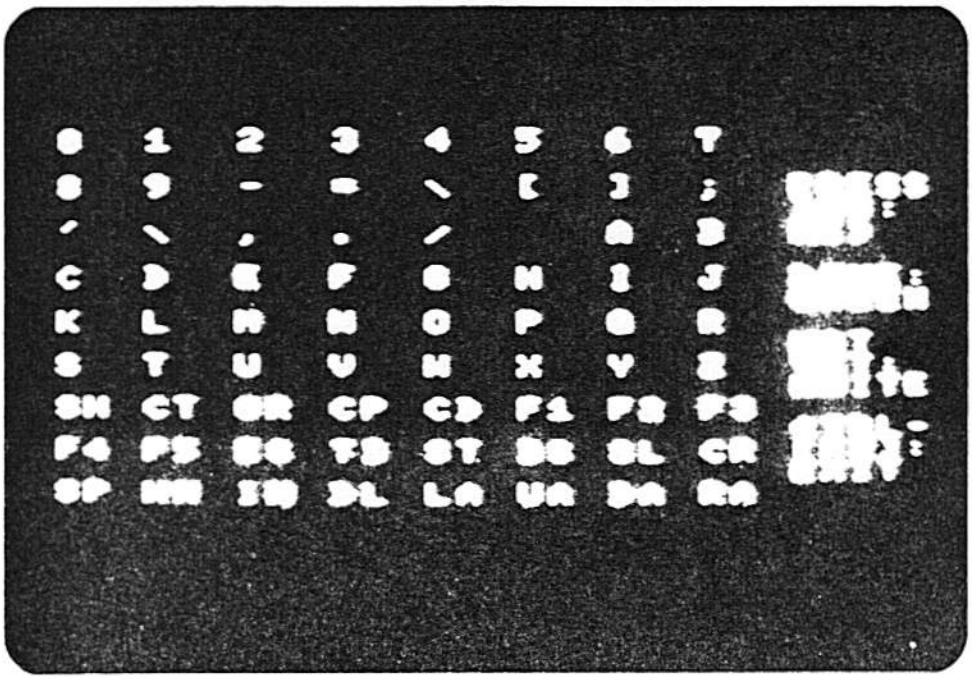


Figure 6.12 Keyboard Test Routine Display

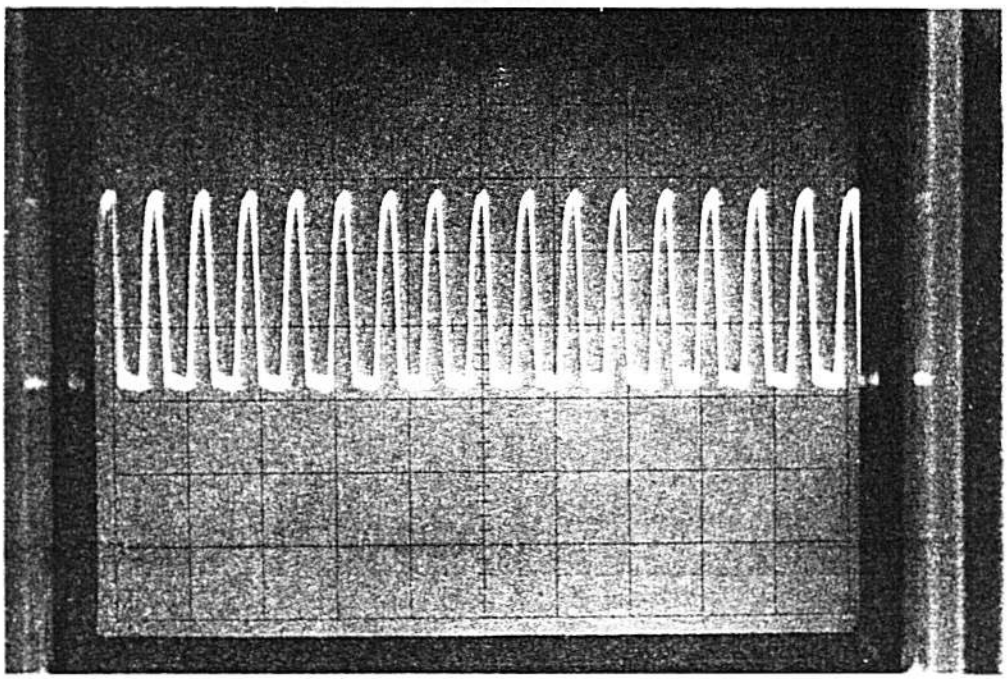


Figure 6.13 FDC Clock Frequency (XT4) 8MHz;
0.2usec/div 0.2v/div

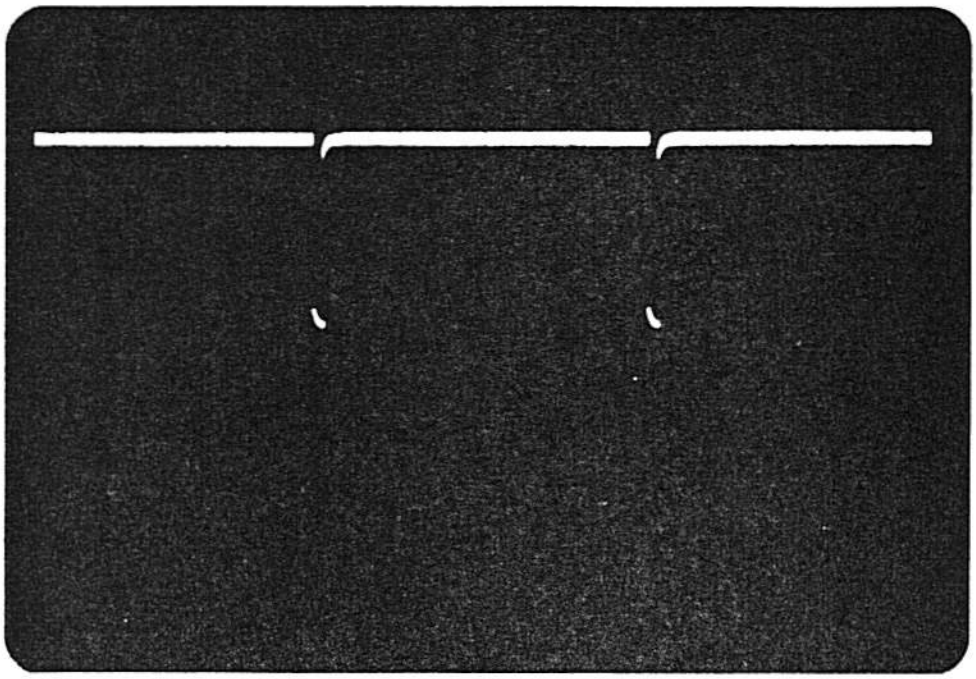


Figure 6.14 CPU $\overline{INT}$ Signal Waveform (TP4); 5msec/div 0.2v/div

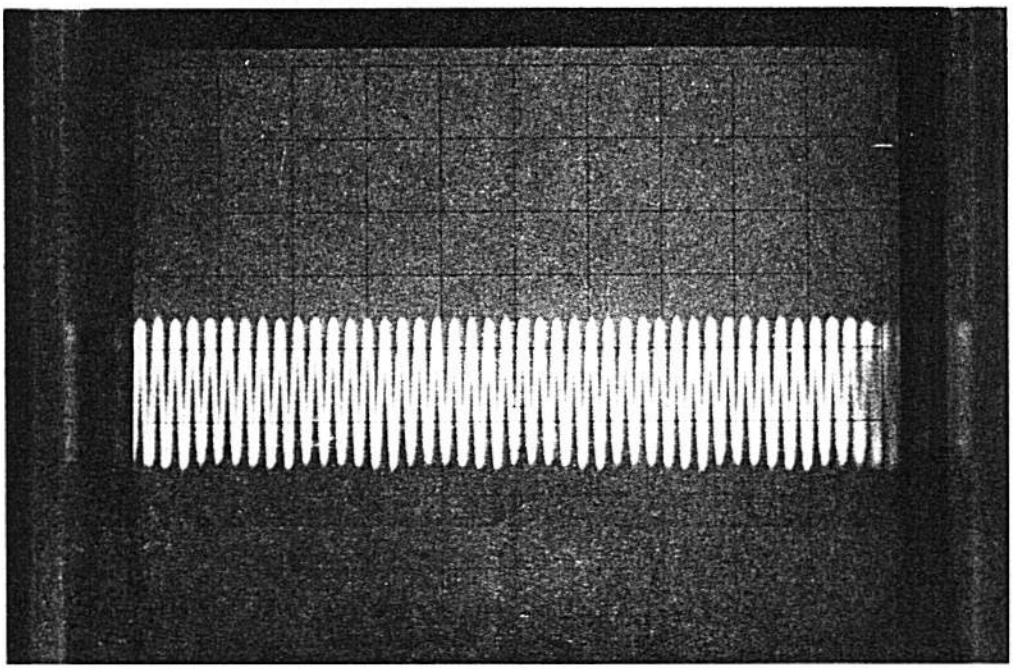


Figure 6.15 MVDP Clock Frequency 21.47727 MHz

APPENDIX A

SPARE PART LIST

A.1 GENERAL RECOMMENDED SPARE PART LIST FOR SVI-738 X'PRESS COMPUTER SYSTEM (PAL VERSION)

Part No.	Description	FOB H.K. US Dollar
IC1488	IC 1488	0.30
IC1489	IC 1489	0.30
IC1793	1793 FDC	4.30
IC311	LM311	0.20
IC31377	RGB PAL INTSC ENCODER	1.40
IC358	LM358	0.30
IC80A	Z80A CPU IC	0.90
IC8251A	8251A USART	1.30
IC8253	8253A PROGRAMMABLE TIMER	1.30
IC8910	AY-3-8910 PSG	2.10
IC9938	9938 MVDP	14.60
ID0001	IN4148:SILICON DIODE	0.10
IG0002	ULA 9RA041	4.60
IG0003	ULA 5RA087	3.30
IL04LS	74LS04	0.20
IL06	7406	0.20
IL07	IC 7407	0.20
IL08LS	74LS08	0.20
IL133LS	74LS133	0.30
IL138LS	74LS138	0.20
IL139LS	74LS139	0.20
IL14LS	IC 74LS14	0.20
IL157LS	74LS157	0.30
IL161LS	IC 74LS161	0.30
IL175LS	74LS175	0.30
IL195LS	74LS195	0.30
IL244LS	74LS244	0.40
IL273LS	74LS273	0.40
IL32LS	74LS32	0.10
IL367LS	74LS367	0.30
IL38	7438	0.20
IL74LS	74LS74	0.20
IM0640030	64K RS232 MASK ROM	1.90
IM1280130	128 DISK MASK ROM	2.80
IM416420	4164 D. RAM 200NS	0.60
IM441612	4416 D. RAM 120NS	1.20
IT0004	TRANSISTOR 9014B	0.10
IT0012	TRANSISTOR 9015B	0.10
JI00202	SLEEV'N TUBE L=2MM D=2MM	0.10
JI01001	SLEEV'N TUBE L5MM D1MM E	0.10
KE3010016	10UF 16V ELECT. CAP.	0.10
KE3047016	47UF 16V ELECT. CAP.	0.10

Part No.	Description	FOB H.K. US Dollar
KE3100016	E.CAP. 100UF 16V	0.10
KE3470025	470UF 25V ELECT. CAP.	0.10
KM110050	0.001UF 50V MAYLAR CAP.	0.10
KM2010050	0.01UF 50V MAYLAR CAP.	0.10
KM2100050	0.1UF MYLAR CAP. 50V	0.10
KR1007050	7PF CERAMIC CAP. 50V	0.10
KR1010050	10PF 50V CERAMIC CAP.	0.10
KR1033050	33PF 50V CERAMIC CAP	0.10
KR1100025	100PF 25V CERAMIC CAP.	0.10
KR1150050	150PF 50V CERAM CAP.	0.10
KR1220050	220PF CERAMIC CAP. 50V	0.10
KR2001050	1000PF CERAMIC CAP. 50V	0.10
KR2010050	0.01UF 50V CERAMIC CAP.	0.10
KR2100025	0.1UF 25V CERAMIC CAP.	0.10
KT1045E	6.8-45P TOP ADJ TRIMCAP	0.10
MC21M477	X'TAL 21.47727 MHZ	0.40
MC3200184S	1.8432 MHZ X'TAL-SMAL	1.30
MC32004	4.433619 MHZ X'TAL	0.50
MC32008	8 MHZ X'TAL	0.50
MJ129	1 WAY WIRE#22 L=150MM BK	0.10
MJ130	1 WAY WIRE#22 L=150MM OR	0.10
MJ131	1 WAY WIRE#22 L-150MM YE	0.10
MJ132	1 WAY WIRE#22 L=150MM RE	0.10
MJ738004	DR CABLE ASS'Y 4-WAY	0.10
MP082	8 PIN DIN SOCKET	0.30
MP091	9 PIN JOYSTICK SOCKET	0.20
MP092	RS-232-C CONNECTOR 9 PIN	1.10
MP142A	14 PIN PRINTER SOCKET	1.10
MP252-2	DRIVE CONNECTOR 25 PIN	1.40
MP282	28 PIN IC SOCKET	0.20
MP341-1	34 PIN D.R. HEADER	0.70
MP502D-1	25/50 SL CARD EDGE CNTR	1.00
MP642	64 PIN IC SOCKET 1.78P	1.10
MS015	5V SPDT RELAY	0.70
RF0103	10 OHM 1/4W +/-5%	0.10
RF0223	22 OHM 1/4W 5% RESISTOR	0.10
RF0753	75 OHM 1/4W 5% RESISTOR	0.10
RF1103	100 OHM 1/4W 5% RESISTOR	0.10
RF1153	150 OHM 1/4W 5% RESISTOR	0.10
RF1203	200 OHM 1/4W +/-5% RSTR	0.10
RF1273	270 OHM 1/4W 5% RESISTOR	0.10
RF1333	330 OHM 1/4W +/-5%	0.10
RF1473	470 OHM 1/4W +/-5%	0.10
RF1513	510 OHM 1/4W +/-5% RSTR	0.10
RF1823	820 OHM RSTR 1/4W 5%	0.10
RF2103	1K OHM 1/4W +/-5%	0.10
RF2203	2.0K 1/4W 5% RESISTOR	0.10
RF2473	4.7K OHM 1/4W +/-5%	0.10
RF2513	5.1K OHM 1/4W 5% RSTR	0.10
RF2563	5.6K OHM 1/4W +/-5%	0.10
RF3103	10K OHM 1/4W +/-5%	0.10
RF3123	12K OHM 1/4W +/-5%	0.10

Part No.	Description	FOB H.K. US Dollar
RF3203	20K OHM 1/4W +/-5%	0.10
RF3563	56K OHM 1/4W +/-5% RSTR	0.10
RF4103	100K OHM 1/4W +/-5%	0.10
RF4473	470K OHM 1/4W +/-5%	0.10
RV3101H	10K OHM VR (H. TYPE)	0.10
SP73802-1	738 MAIN BOARD VER 2.1	11.60
TC0001	10UF CHOKE COIL	0.10
XC73803	RCA SOCKET V/A	0.20
XC73811	HEAT SINK PLATE (VDP)	0.10
FF0002	2A MINI FUSE MEDIAN	0.10
FS0003	FUSE CHIP FOR D=5MM FUSE	0.10
IA7812CT	12V REGULATOR 2A TO-220	0.30
IA7912CT	-12V REGULATOR TO-220	0.30
ICL4964	ICL4964 SWITCHING REG.	3.00
ID0002	RECTIFIER DIODE 3A	0.10
ID0006	IN5822 SWITCHING DIODE	0.40
ID581904	IN5819 SWITCHING DIODE	0.30
JI04515	SLEEV'N TUBE L=14 D=1.5	0.10
KE14702501	SW. REG CAP. 470UF 25V	0.30
KE22200050	2.2UF 50V ELECT. CAP.	0.10
KE3100016	E. CAP. 100UF 16V	0.10
KE3100025	100UF 25V ELECT. CAP.	0.10
KE3100025S	SW. REG CAP. 100UF 25V	0.20
KE32200025	2200UF 25V E-CAP	0.30
KM120050	0.002UF 50V MYLAR CAP.	0.10
KM2033100	.033UF 100V MYLAR CAP.	0.10
KM2100050	0.1UF MYLAR CAP. 50V	0.10
MP024	POWER JACK KB11-0075	0.20
MS006	POWER SWITCH 3P2T	0.20
RF1513	510 OHM 1/4W +/-5% RSTR	0.10
RF2103	1K OHM 1/4W +/-5%	0.10
RF2433	4.3K OHM 1/4W +/-5% RSTR	0.10
RF3153	15K OHM 1/4W +/-5% RESIST	0.10
SP73804-1	POWER PCB VER 2.0	0.30
TC0010	TOROI COIL 90UH	0.30
TC0011	TOROI COIL 360/970UH	1.90
XC73808	738 HEAT SINK	0.60
XS039	S.T.SCREW D3X14 BLACK	0.10
XS054	MS/PH SCREW M3X0.5PX8	0.10
MJ738003	DR CABLE ASS'Y 34-WAY	2.00
MR020003	CUSHION FOR DISK DRIVE	0.10
WA73801	MSX LABEL	0.10
WN73801	CABINET TOP	1.00
WN73802	CABINET BOTTOM	1.60
WN73807	LEFT COVER PLATE	0.10
WN73808	RIGHT COVER PLATE	0.10
WN73809	TOP HANDLE BAR	0.20
WN73810	BOTTOM HANDLE BAR	0.20
WN73811	LEFT HANDLE ARM	0.10
WN73812	RIGHT HANDLE ARM	0.10
WN73813	CARTRIDGE HOUSING	0.20
WN73814	CARTRIDGE DOOR	0.10

Part No.	Description	FOB H.K. US Dollar
WN73817	HANDLE FOOT	0.10
XC020115	ODIOXID3.3X0.7 WASHER	0.10
XC603-5	DOOR SPRING	0.10
XC73802	MOUNTING BRACKET	0.10
XC73807	SVI LOGO NAME PLATE	0.10
XC73812	SPACER FOR DRIVER	0.10
XS044	M.SCREW M3XP0.5X6	0.10
XS059	MS/PH SCREW M3X0.5PX5	0.10
XS062	M.SCREW, M3X0.5X10	0.10
XS085	S.T. SCREW P3 X 8 BT	0.10
XS086	SCREW F.M3 X 10 X 0.5P	0.10
XS088	S.T. SCREW B 3 X 12 BT	0.10
XS090	ST.SCREW F3X10 AB N1.PL	0.10
[illegible]	[illegible]	[illegible]
DL003	2X5 LED RED	0.10
DL012	LED	0.10
ID0001	IN4148:SILICON DIODE	0.10
MJ009	12 WIRE CONNECTOR	0.10
SP73801-1	738 KEYBOARD SINGLE SIDE	3.10
WN328003	SPACE BAR GUIDE PLATE	0.10
WN73803	KEY FRAME	1.10
WN73805	PUSH BUTTON	0.10
WN73806	KEY SHAFT	0.10
WN73815	RUBBER CONNECTOR	2.00
XC328001	SPACE BAR SPRING	0.10
XC328002	SPACE BAR METAL BAR	0.10
XS060	S.T.SCREW D2.0 X 8.0	0.10
**IM2560130	256K MSX ROM DIN	3.90
MJ030	PCA-PAL 75 OHM CABLE	0.50
*MM004	UM1286-2 U,591.25/5.5	3.40
*TP259-1	220/16V AC VDE ADAPTOR	5.50
**WN73804-1	KEY TOP SET 69 KEYS (GI)	4.00
PB318101-M	SILICA GEL BAG SMALL	0.10
PC738101-1	MASTER CARTON (3 INI)	0.50
PG738001-1	GIFT BOX	1.40
PG738004	CARRYING CASE SPACER	0.10
PI318104(S)	GUARANTEE CARD (SVI)	0.10
PI738001	EXPRESS USER'S MANUAL	1.10
PI738002	MSX DOS MANUAL	0.80
PI738003	MSX DISK BASIC MANUAL	0.40
PI738004	MSX BASIC MANUAL	1.00
PI738006	CP/M USER'S MANUAL	0.90
PI738102	ENHANCEMENT FRO SVI-738	0.10
PIBW020102	END USER LICENSE	0.10
PIBW020103	DIGITAL REPLY CARD	0.10
PP73801-1	POLYFOAM CAP. (80'C)	1.10
PZ020101	PVC BAG FOR 02 UNIT	0.10
PZ020104	PVC BAG FOR MANUALS	0.10
PZ738005	A CARRYING BAG	9.50
WA003-2	QC PASSED LABEL (GOLDEN)	0.10
WA062	CARTON LABEL	0.10
WA067	COLOR LABEL (P)	0.10

Part No.	Description	FOB H.K. US Dollar
WA133	SERIAL NO. LABEL-738	0.10
WA73802-1	CP/M 2.2 LAB	0.10
WA73802-3	MSX DOS/DISK BASIC LAB	0.10
WA73804	AN ID LABEL	0.10
WN73818	COVER SHEET	0.10
ZDBW0201	3.5" BLANK DISKETTE	1.70

* Different part no. and price for TV modular and power adaptor may be used in different countries.

** This items may depend on language version used.

N.B. Price is subject to change without prior notice.

Part No.	Description	FOB H.K. US Dollar
KR1150050	150PF 50V CERAM CAP.	0.10
KR1220050	220PF CERAMIC CAP. 50V	0.10
KR2001050	1000PF CERAMIC CAP. 50V	0.10
KR2010050	0.01UF 50V CERAMIC CAP.	0.10
KR2100025	0.1UF 25V CERAMIC CAP.	0.10
KT1045E	6.8-45P TOP ADJ TRIMCAP	0.10
MC21M477	X'TAL 21.47727 MHZ	0.40
MC3200184S	1.8432 MHZ X'TAL-SMAL	1.30
MC32004	4.433619 MHZ X'TAL	0.50
MC32008	8 MHZ X'TAL	0.50
MJ129	1 WAY WIRE#22 L=150MM BK	0.10
MJ130	1 WAY WIRE#22 L=150MM OR	0.10
MJ131	1 WAY WIRE#22 L=150MM YE	0.10
MJ132	1 WAY WIRE#22 L=150MM RE	0.10
MJ738004	DR CABLE ASS'Y 4-WAY	0.10
MP082	8 PIN DIN SOCKET	0.30
MP091	9 PIN JOYSTICK SOCKET	0.20
MP092	RS-232-C CONNECTOR 9 PIN	1.10
MP142A	14 PIN PRINTER SOCKET	1.10
MP252-2	DRIVE CONNECTOR 25 PIN	1.40
MP282	28 PIN IC SOCKET	0.20
MP341-1	34 PIN D.R. HEADER	0.70
MP502D-1	25/50 SL CARD EDGE CNTR	1.00
MP642	64 PIN IC SOCKET 1.78P	1.10
MS015	5V SPDT RELAY	0.70
RF0103	10 OHM 1/4W +/-5%	0.10
RF0223	22 OHM 1/4W 5% RESISTOR	0.10
RF0753	75 OHM 1/4W 5% RESISTOR	0.10
RF1103	100 OHM 1/4 5% RESISTOR	0.10
RF1153	150 OHM 1/4W 5% RESISTOR	0.10
RF1203	200 OHM 1/4W +/-5% RSTR	0.10
RF1273	270 OHM 1/4W 5% RESISTOR	0.10
RF1333	330 OHM 1/4W +/-5%	0.10
RF1473	470 OHM 1/4W +/-5%	0.10
RF1513	510 OHM 1/4W +/-5% RSTR	0.10
RF1823	820 OHM RSTR 1/4W 5%	0.10
RF2103	1K OHM 1/4W +/-5%	0.10
RF2203	2.0K 1/4W 5% RESISTOR	0.10
RF2473	4.7K OHM 1/4W +/-5%	0.10
RF2513	5.1K OHM 1/4W 5% RSTR	0.10
RF2563	5.6K OHM 1/4W +/-5%	0.10
RF3103	10K OHM 1/4W +/-5%	0.10
RF3123	12K OHM 1/4W +/-5%	0.10
RF3203	20K OHM 1/4W +/-5%	0.10
RF3563	56K OHM 1/4W +/-5% RSTR	0.10
RF4103	100K OHM 1/4W +/-5%	0.10
RF4473	470K OHM 1/4W +/-5%	0.10
RV3101H	10K OHM VR (H. TYPE)	0.10
SP73802-1	738 MAIN BOARD VER 2.1	11.60
TC0001	10UF CHOKE COIL	0.10
XC73803	RCA SOCKET V/A	0.20
XC73811	HEAT SINK PLATE (VDP)	0.10
FF0002	ZA MINI FUSE MEDIAN	0.10
FS0003	FUSE CHIP FOR D=5MM FUSE	0.10

Part No.	Description	FOB H.K. US Dollar
IA7812CT	12V REGULATOR 2A TO-220	0.30
IA7912CT	-12V REGULATOR TO-220	0.30
ICL4964	ICL4964 SWITCHING REG.	3.00
ID0002	RECTIFIER DIODE 3A	0.10
ID0006	IN5822 SWITCHING DIODE	0.40
ID581904	IN5819 SWITCHING DIODE	0.30
JI04515	SLEEV'N TUBE L=14 D=1.5	0.10
KE14702501	SW. REG CAP. 470UF 25V	0.30
KE22200050	2.2UF 50V ELECT. CAP.	0.10
KE3100016	E. CAP. 100UF 16V	0.10
KE3100025	100UF 25V ELECT. CAP.	0.10
KE3100025S	SW.REG CAP. 100UF 25V	0.20
KE32200025	2200UF 25V E-CAP.	0.30
KM120050	0.002UF 50V MAYLAR CAP.	0.10
KM2033100	.033UF 100V MAYLAR CAP.	0.10
KM2100050	0.1UF MYLAR CAP. 50V	0.10
MP024	POWER JACK KB11-0075	0.20
MS006	POWER SWITCH 3P2T	0.20
RF1513	510 OHM 1/4W +/-5% RSTR	0.10
RF2103	1K OHM 1/4W +/-5%	0.10
RF2433	4.3K OHM 1/4W +/-5% RSTR	0.10
RF3153	15K OHM 1/4W +/-5% RESIST	0.10
SP73804-1	POWER PCB VER 2.0	0.30
TC0010	TOROI COIL 90UH	0.30
TC0011	TOROI COIL 360/970UH	1.90
XC73808	738 HEAT SINK	0.60
XS039	S.T.SCREW D3X14 BLACK	0.10
XS054	MS/PH SCREW M3X0.5PX8	0.10
MJ738003	DR CABLE ASS'Y 34-WAY	2.00
MR020003	CUSHION FOR DISK DRIVE	0.10
WA73801	MSX LABEL	0.10
WN73801	CABINET TOP	1.00
WN73802	CABINET BOTTOM	1.60
WN73807	LEFT COVER PLATE	0.10
WN73808	RIGHT COVER PLATE	0.10
WN73809	TOP HANDLE BAR	0.20
WN73810	BOTTOM HANDLE BAR	0.20
WN73811	LEFT HANDLE ARM	0.10
WN73812	RIGHT HANDLE ARM	0.10
WN73813	CARTRIDGE HOUSING	0.20
WN73814	CARTRIDGE DOOR	0.10
WN73817	HANDLE FOOT	0.10
XC020115	ODIOXID3.3X0.7 WASHER	0.10
XC603-5	DOOR SPRING	0.10
XC73802	MOUNTING BRACKET	0.10
XC73807	SVI LOGO NAME PLATE	0.10
XC73812	SPACER FOR DRIVER	0.10
XS044	M.SCREW M3XP0.5X6	0.10
XS059	MS/PH SCREW M3X0.5PX5	0.10
XS062	M.SCREW, M3X0.5X10	0.10
XS085	S.T. SCREW P3 X 8 BT	0.10
XS086	SCREW F.M3 X 10 X 0.5P	0.10
XS088	S.T. SCREW B 3 X 12 BT	0.10
XS090	ST.SCREW F3X10 AB N1.PL	0.10

Part No.	Description	FOB H.K. US Dollar
YS73801	F353 3.5" DRIVE	62.50
DL003	2X5 LED RED	0.10
DL012	LED	0.10
ID0001	IN4148:SILICON DIODE	0.10
MJ009	12 WIRE CONNECTOR	0.10
SP73801-1	738 KEYBOARD SINGLE SIDE	3.10
WN328003	SPACE BAR GUIDE PLATE	0.10
WN73803	KEY FRAME	1.10
WN73805	PUSH BUTTON	0.10
WN73806	KEY SHAFT	0.10
WN73815	RUBBER CONNECTOR	2.00
XC328001	SPACE BAR SPRING	0.10
XC328002	SPACE BAR METAL BAR	0.10
XS060	S.T.SCREW D2.0 X 8.0	0.10
KR2010050	0.01UF 50V CERAMIC CAP	0.10
MC32003	3.579545 MHZ X'TAL	0.40
*MM005	UM1285-8,V,61,67.7/4.5	3.40
MS008	MODULATOR SWITCH	0.20
*TP258-1	120/16V AC UL ADAPTOR	4.80
WA73803	AN ADAPTOR LABEL	0.10
PB318101-M	SILICA GEL BAG SMALL	0.10
PC738101-1	MASTER CARTON (3 INI)	0.50
PG738001-1	GIFT BOX	1.40
PG738004	CARRYING CASE SPACER	0.10
PI318104(S)	GUARANTEE CARD (SVI)	0.10
PI738001	EXPRESS USER'S MANUAL	1.10
PI738002	MSX DOS MANUAL	0.80
PI738003	MSX DISK BASIC MANUAL	0.40
PI738004	MSX BASIC MANUAL	1.00
PI738006	CP/M USER'S MANUAL	0.90
PI738102	ENHANCEMENT FRO SVI-738	0.10
PIBW020102	END USER LICENSE	0.10
PIBW020103	DIGITAL REPLY CARD	0.10
PP73801-1	POLYFOAM CAP. (80'C)	1.10
PZ020101	PVC BAG FOR 02 UNIT	0.10
PZ020104	PVC BAG FOR MANUALS	0.10
PZ738005	A CARRYING BAG	9.50
WA003-2	QC PASSED LABEL (GOLDEN)	0.10
WA062	CARTON LABEL	0.10
WA067	COLOR LABEL (P)	0.10
WA133	SERIAL NO. LABEL-738	0.10
WA73802-1	CP/M 2.2 LAB	0.10
WA73802-3	MSX DOS/DISK BASIC LAB	0.10
WA73804	AN ID LABEL	0.10
WN73818	COVER SHEET	0.10
ZDBW0201	3.5" BLANK DISKETTE	1.70

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